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2018-1768

IN THE
UNITED STATES COURT OF APPEALS FOR
THE FEDERAL CIRCUIT

POLARIS INNOVATIONS LIMITED,
Appellant

v.

KINGSTON TECHNOLOGY COMPANY, INC.
Appellee

APPEAL FROM THE UNITED STATES PATENT AND TRADEMARK OFFICE, PATENT TRIAL AND APPEAL BOARD NO. IPR2016-01621

PRINCIPAL BRIEF OF APPELLANT POLARIS INNOVATIONS LIMITED

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July 10, 2018

CERTIFICATE OF INTEREST

Counsel for Appellant Polaris Innovations Limited ("Polaris") in Appeal No. 2018-1768 certifies the following:

1. The full name of every party or amicus represented by me is:

Polaris Innovations Limited.

2. The name of the real party in interest (if the party named in the caption is not the real party in interest) represented by me is:

Quarterhill Inc.

3. All parent corporations and any publicly held companies that own 10 percent or more of the stock of the party or amicus curiae represented by me are:

Wi-LAN, Inc.

4. The names of all law firms and the partners or associates that appeared for the party or amicus now represented by me in the trial court or agency or are expected to appear in this court are:

Parham Hendifar, Lowenstein & Weatherwax LLP

5. The title and number of any case known to counsel to be pending in this or any other court or agency that will directly affect or be directly affected by this court's decision in the pending appeal are:

- *Polaris Innovations Limited v. Kingston Technology Company, Inc.*, 8:16-cv-00300 (C.D. Cal).

Dated: July 10, 2018

/s/ Matthew D. Powers
Matthew D. Powers

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STATEMENT OF RELATED CASES

No appeal from this Inter Partes Review ("IPR") has previously been before this Court or any other court.

The Court has identified *sua sponte* the following appeals as companion cases to this appeal, to be assigned to the same merits panel and argued on the same day as the present appeal:

- *Kingston Technology Company, Inc*. v. *Polaris Innovations Limited*, No. 18-1778 (Fed. Cir.)
- *Polaris Innovations Limited* v. *Kingston Technology Company, Inc*., No. 18-1831 (Fed. Cir.).

The following pending action will be directly affected by this Court's decision in this appeal: *Polaris Innovations Limited* v. *Kingston Technology Company, Inc*., 8:16-cv-300 (C.D. Cal.). That case is currently stayed pending resolution of IPR proceedings, including among others the IPR that is the subject of this appeal and the IPRs that are the subject of the two companion cases listed above.

I. STATEMENT OF JURISDICTION

The Patent Trial and Appeal Board ("PTAB" or "Board") of the United States Patent and Trademark Office ("USPTO") issued its Final Written Decision in the *Inter Partes* Review ("IPR") under 35 U.S.C. § 318(a) on January 29, 2018. Appx1-44. Polaris filed a timely notice of appeal under 35 U.S.C. §§ 141(c), 142 and 319 on April 2, 2018. Appx514-519. This Court has jurisdiction under 35 U.S.C. § 141(c) and 28 U.S.C. § 1295(a)(4)(A). The decision appealed from is final.

II. STATEMENT OF THE ISSUES

Whether the Board's opinion that Claims 1–17 of the U.S. Patent No. 6,438,057 ("057 Patent") are obvious should be reversed or vacated where:

1. The Board erred by adopting an unreasonably broad, implicit construction of the "signal indicative of [a] temperature of the DRAM array" limitation found in all challenged claims;

2. The Board erred by crafting, in its decision on institution of review, a new ground of unpatentability not identified in the Petition to find Claims 2, 4, 10–11, 14–15, and 17 ("the diode claims") obvious;

3. The Board erred by basing its unpatentability determination on factual findings unsupported by substantial evidence for all challenged claims; and

4. The cancellation of Polaris's claims violated the Appointments Clause of the Constitution as a final agency decision requiring the Board to act as "principal

Officers" without having been appointed by the President and confirmed by the Senate.

III. STATEMENT OF THE CASE AND FACTS

A. Introduction

Polaris appeals the Board's Final Written Decision (Appx1-44) in the IPR that all seventeen challenged claims of Polaris's 057 patent are unpatentable. In this IPR proceeding, the Board's conclusion that Polaris's patent claims should be cancelled rests on a foundation of erroneous implicit claim construction; grounds of institution that were lacking from the petition, created by the Board, and only addressed on the merits by Kingston after all substantive written submissions from Polaris had been spent; and factual determinations on the merits that were not based on substantial evidence. Each of these errors must be corrected on appeal. Further, even holding these errors to one side, the IPR decision cancelling Polaris's patent rights was a violation of the Appointments Clause of the United States Constitution because it requires the Board to act as principal Officers even though they were never appointed by the President, by and with the advice and consent of the Senate. This Court should restore Polaris's rights.

B. The 057 Patent

The 057 patent is directed to improvements in dynamic random access memory, or DRAM. Appx598 (1:5-10). DRAM uses stored voltages to store data

bits in arrays. Appx598 (1:46-51). DRAM is the universally dominant form of computer main memory because of its low cost due to its simple structure and dramatically lower number of components than alternatives. Appx1094 (¶ 43). But the unique, low-cost structure that gives DRAM its advantage, has attendant disadvantages, which have given rise to a long-felt need for ways to alleviate them. Appx598 (1:63-2:2); Appx1088-1089 (¶ 36); Appx1094 (¶ 43). A critical disadvantage of DRAM is that the data bits stored on its array are not permanent. Appx54. "Leakage" from its relatively simple, inexpensive arrays of storage circuits, means the stored bits only last a few microseconds and are then lost or corrupted unless their voltage is "refreshed," *i.e.*, rewritten periodically. Appx598 (1:51-59); Appx1088-1089 (¶ 36). This refresh process may be implemented internally, as "self refresh," where "the DRAM itself set the refresh timing," or externally, where for example, an external chipset issues a refresh command to the DRAM array via a connection pin. Appx598 (1:63-2:2); Appx1088-1089 (¶ 36).

The need for continual refresh creates continual power dissipation, with attendant difficulties of temperature increase and reduced efficiency. Appx598 (2:4-14); Appx1090 (¶ 38). Because a refresh cycle includes discharging and then recharging every cell in the DRAM device, the power dissipation associated with that step is proportional to the refresh rate. Appx1088 (¶ 36).

Furthermore, because refresh is necessary to avoid loss of stored data, it can take priority over routine reading and writing cycles, and therefore can seriously reduce "the bandwidth (e.g., data throughput) of the overall system in which the DRAM array [] is utilized." Appx598 (2:15-20); Appx1088-1089 (¶ 36). The more often the DRAM is occupied with refresh cycles, the less data throughput is available between the DRAM memory and the system utilizing it. *Id*.; Appx599 (3:58-60).

The rate of refresh necessary to reliably preserve stored data in DRAM varies with the temperature, so "when the temperature of the DRAM array is relatively high, a correspondingly high refresh rate . . . may be required to ensure integrity of the data stored in the DRAM array." Appx599 (3:55-58).

The 057 patent's inventor recognized that a significant source of DRAM's disadvantages was that conventional DRAM arrays used a high refresh rate, "based on a worst-case high temperature condition," to guard against data loss by compensating for the dependence of the necessary refresh rate on the array temperature. Appx598 (1:59-62); Appx599 (3:52-66); Appx1089-1090 (¶ 37). The inventor realized that if the temperature of the DRAM array is known to be lower than that worst-case value, a correspondingly lower refresh rate may be utilized that will ensure data integrity with lower power, higher overall system bandwidth, and more performance. Appx599 (3:60-66); Appx1089-1091 (¶¶ 37-39).

To exploit the temperature dependence of the required refresh rate to reduce power consumption and increase performance in an acceptable tradeoff with added components and complexity, the 057 patent discloses a novel invention.

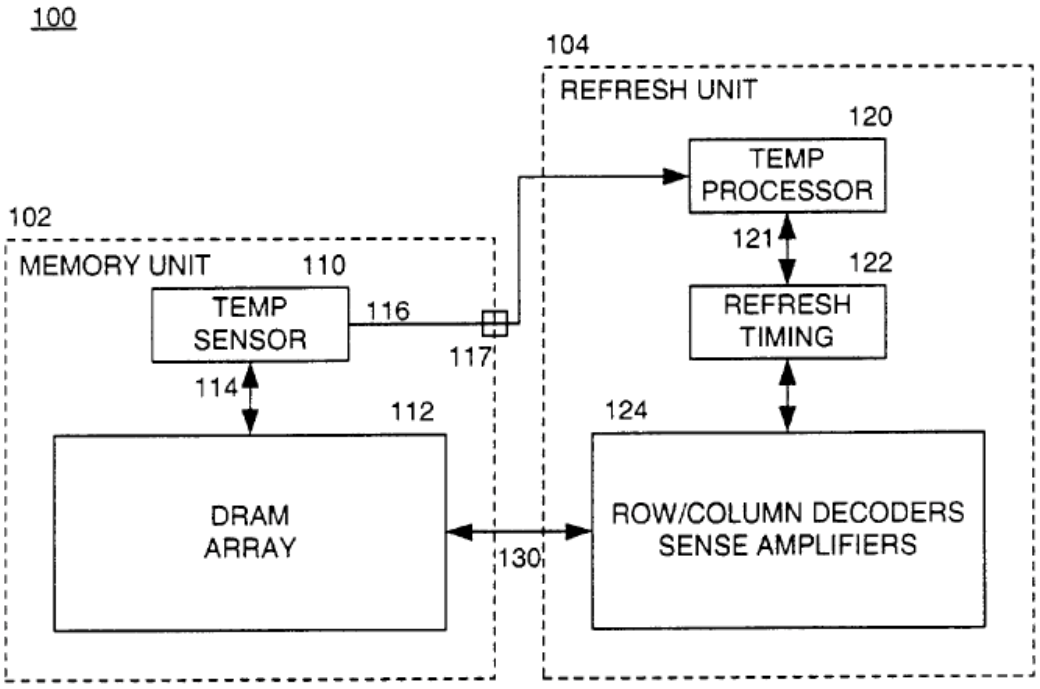

FIG. 3

As shown in Figure 3 (Appx595), the 057 patent describes, *e.g.*, a semiconductor package (102) including at least one connection pin (117); a DRAM array (112) disposed within the package (102); and a temperature sensor (110) in thermal communication with the array (112), which is operable to produce a signal indicative of the array's temperature (116), and is coupled to the pin (117) such that the signal may be provided to external circuitry (e.g., 104), wherein the array (112)

is refreshed at a rate that decreases and increases as the temperature of the array decreases and increases, respectively. *Id*., Appx598-600 (1:66-2:2, 2:26-37, 2:63-67, 4:18-22, 4:30-37, 4:48-53, 5:37-48, 5:60-6:7). The sensor (110) may include a diode having a forward voltage drop that varies as a function of the array's temperature so the signal corresponds to the voltage drop. *Id*.; Appx598; Appx600 (2:38-42, 2:59-62, 6:8-12); Appx1119-1120 (¶ 102).

The 057 patent allows a lower DRAM array refresh rate to be utilized during normal operation while ensuring data integrity, with the rate being increased when the temperature of the array is sensed to have increased, and decreased when the temperature of the array is sensed to have decreased, and yet does not require corresponding adjustment of the refresh rate to be implemented internally. Appx1093-1094 (¶ 42).

Because the temperature sensor and the DRAM array are disposed in a semiconductor package including at least one connection pin operable to provide the signal indicative of the temperature of the array to external circuitry, the refresh function may be performed by external circuitry during operation of the overall system. Appx599 (4:48-57); Appx1091-1093 (¶¶ 40-41).

The claimed invention not only helped meet a long-felt need to alleviate the power dissipation and efficiency disadvantages of DRAM, it achieved unexpected

results, including one unexpected even to the inventor. Appx599 (3:64-4:10); Appx1110-1111 (¶ 82); Appx1288-1289 (165:11-166:11).

First, the claimed invention can react to an increase in the operating temperature of the array by taking actions (*i.e.*, increasing the refresh rate) that increase the temperature and increase the rate of energy consumption of the array and associated circuitry, and the thermal stress on the DRAM most when the array is at its hottest. Appx598 (1:19-21 and 2:3-12); Appx599 (3:58-4:10); Appx1093-1094 (¶ 42). Although this is a counterintuitive strategy for reducing overall array power consumption while maintaining reliability, a core principle of the invention is that it increases overall efficiency, by permitting a relatively lower refresh rate overall during operation under moderate temperatures, because it can permit a lower overall DRAM refresh rate during less active cycles compared to the relatively high conventional manufacturer-established, worst-case refresh rate. *Id.*; Appx598 (2:3-15); Appx599 (3:52-66); Appx1093-1094 (¶ 42).

Second, in DRAM technology the 057 patent's very goal—improving performance and power efficiency simultaneously—itself is nonobvious. Appx598 (2:3-24); Appx1094-1095 (¶ 44). As Kingston's expert admitted, in DRAM "if you are trying to improve performance, it's usually at the cost of energy all else being equal." Appx1203 (229:20-25); Appx1094-1095 (¶ 44). Yet the 057 patent explicitly

stated—and accomplished—the goal of doing both simultaneously. Appx598 (2:3-24).

Third, the invention provided synergy within the framework of the very rapid paradigm shift in the computer industry from asynchronous to synchronous system memory that occurred soon after the invention. Appx1095-1096 (¶ 45); Appx1110-1111 (¶ 82); Appx1161 (59:13-17); Appx1162 (62:5-8); Appx1275 (112:8-113:11). A characteristic of the paradigm shift to "synchronous" DRAM ("SDRAM"), and now DDR (Double Data Rate), dominating the DRAM market, is that the DRAM's operation, including its refresh cycles, may be controlled according to the ***external*** system clock, making the refresh, from the system's perspective, deterministic, and permitting the system to both adjust refresh rates to keep them only as high as needed and coordinate that refresh rate with external data traffic needs of transferring data to the memory blocks. Appx1095-1096 (¶ 45)

Prior to SDRAM paradigm shift, normal (non-synchronous) DRAM was limited in its access time by its internal wiring and transistor speeds. Appx1096 (¶ 47). As integrated circuit technology progressed, internal circuit speeds now far exceed external communication speeds and the industry has found that the clock speed in the DRAM should be better controlled from outside the chip, to let the board or system designer provide the fastest possible external circuits and synchronize the

external bus with each DRAM since the board signal delays now dominate data transfer to the chips. *Id*. (¶¶ 46-47)

Hence, it is now found that synchronization is best handled off the chip. *Id*. Before SDRAM took the industry by storm, it would not have been obvious to add an external pin to facilitate such synchronization because of the increased complexity of placement and routing, nor would it have been obvious to place (as in the 057) an onboard sensor to generate a temperature indicative signal for external provision. *Id*.; Appx1096-1097 (¶ 48).

One particular opportune result of this paradigm shift, however, is that SDRAM that uses the claimed invention synergistically improves both the memory's effective performance, and in the 057 patent's terms its bandwidth, by externally controlling the timing of the refresh to coordinate it with read and write cycles based on the interactively monitored needs of the chips and adjustment during operation based on the internal temperature of the DRAM array. Appx1094-1096 (¶¶ 44-45); Appx1275 (112:8-23).

C. The *Inter Partes* Review

Appellee Kingston filed an IPR petition seeking review of Claims 1–17 of the 057 patent. Appx45-115. Kingston challenged all claims as obvious on the following four grounds:

Ground 1:	§ 103 in view of Atkinson	Renders claims 1-17 obvious for § 103(a)
Ground 2:	§ 103 in view of Atkinson and Broadwater	Renders claims 1-17 obvious for § 103(a)
Ground 3	§103 in view of Tillinghast and Broadwater	Renders claims 1-17 obvious for § 103(a)
Ground 4	§103 in view of Kodama and Lee '970 or Broadwater	Renders claims 1-17 obvious for § 103(a)

See Appx60-61. Kingston also included a list of prior art references, which included references cited in the four grounds ("Atkinson," "Broadwater," "Tillinghast," "Kodama," and "Lee '970") and two additional references, "JPS499" and the "Kagenishi paper." Appx61-62. More importantly, Kingston did not identify Miller (U.S. Patent No. 3,812,717) or Suzuki (U.S. Patent No. 6,134,667) anywhere in the Proposed Grounds of Unpatentability. Appx60-62.

With respect to Ground 1 based on Atkinson, the Petition referred to Miller only once as an example of the supposed evidence of the finite number of alternatives.[1] Appx71. Ground 2 made no mention of Miller at all.

Atkinson is devoted to self-refresh of DRAM during sleep mode. In normal, active, operational mode, when data is constantly read and written to the memory, there is no motivation to have a "slow" refresh circuit that is controlled internally. Appx1098 (¶¶ 51-53). When the overall system is in "suspended operation," however, the circuitry external to the DRAM is sleeping and frozen, and the system clock is off. Appx891 (6:5-11); Appx895 (14:10-31); Appx900 (23:43-46, 24:22-28, 24:40-44); Appx1098 (¶¶ 51-53). Atkinson is designed to maintain the refresh clock of the DRAM internally, for "self-refreshing" "during suspended operation." Appx900 (24:22-28); Appx1269 (87:23-88:18). Every embodiment of Atkinson is directed to "self-refreshing" during such suspended operation, when the system clock is off and the system is frozen. *Id*. Atkinson prefers to rely on empirical analyses of the typical rate of cooling of DRAM when the system is in sleep mode. *Id*.; Appx891-892 (6:30-46, 6:63-7:19, 7:20-31). In a few non-preferred embodiments, Atkinson has a temperature sensor onboard the DRAM. *Id*.; *see also*

[1] The IPR petition references Miller only five times, and the first two are typographical errors. *See* Appx69 (twice, but quoting from Ex. 1014, which is Suzuki, not Miller); Appx71; Appx91; Appx105. Polaris raised this error, Appx236, but the Board continued to rely on Miller, not Suzuki.

Appx892 (7:32-53); Appx898 (20:64-67); Appx899 (22:39-41); Appx900 (23:30-43). But even then, as the Petition admits, Atkinson does not provide signals indicative of the array temperature to external circuitry via a connection pin. Appx68. Nor could it: when Atkinson's invention is operating, everything else in the system is shut off, and there is nothing to which to communicate this information. Appx1099-1100 (¶ 55).

Kingston argued that Atkinson is directed to reducing battery drain and varying refresh according to temperature. Appx688 (¶ 38). But Atkinson is directed to these goals during suspended operation only. Appx895 (13:11-18) ("During low power modes, the present invention advantageously refreshes memory at a slower rate than during normal operation."); Appx900 (23:43-46, 23:65-67, 24:40-47); Appx1098 (¶¶ 51-52). Unlike the 057 patent, Appx598 (2:32-34), Atkinson does not permit reducing the default rate of DRAM refresh during operation. Instead, Atkinson takes the default operational rate of refresh as a given (or "reference" rate), and proposes a technique for saving energy only during ***non***-operation by cutting the rate of refresh below the high default operational level. *Id*. Appx891 (6:5-11, 6:14-26); Appx1098-1099 (¶ 54).

Thus, Atkinson is intended to operate only in low-temperature shutdown situations when the chips are expected to be cooler than normal operating temperature—and indeed when they would be expected to involve two or three

orders of magnitude less power dissipation than normal operation. Appx1092-1093 (¶ 41); Appx1098-1099 (¶ 54); Appx1109-1110 (¶¶ 80-81).

Broadwater, by contrast, is directed to detecting and reducing the effects of thermal stress on packaged semiconductor chips "such as . . . the control systems of high-speed aircraft" to promote their continued reliable operation by preventing an excess rise in temperature. Appx741 (1:25-29, 1:46-51); Appx30; Appx1100 (¶ 56). Broadwater makes no mention of memory, DRAM, or DRAM refresh. Unlike the 057 patent's DRAM refresh invention, which responds to increasing temperature in the DRAM array by increasing the refresh rate to prevent data loss, and therefore increasing circuit activity and heat dissipation in the array (*see, e.g.*, Appx598 (1:51-59); Appx1106 (¶ 73)), Broadwater responds to increased temperature in its circuitry by shutting circuitry down to reduce temperature increase from the circuits' activity. Appx741 (1:14-45); Appx742 (3:48-64); Appx743 (5:21-27); Appx1100-1101 (¶ 57); Appx1106 (¶¶ 71, 73); Appx1280 (133:1-8). Kingston proposed to combine Atkinson with Broadwater for only one purpose: adding Broadwater's connection pin for provision of a temperature-related signal to external circuitry. Appx80.

Polaris filed a Preliminary Response, pointing out reasons why each ground Kingston identified in the Petition was deficient. Appx116-178.

The Board granted review based on only one of the four grounds identified in the Petition. Kingston's second ground sought review of Claims 1-17 based on

obviousness over "Atkinson and Broadwater." The Board instituted review on that ground of Claims 1, 3, 5–9, 12, 13, and 16 only. Appx199. The Board instituted review of the remaining challenged Claims 2, 4, 10, 11, 14, 15, and 17 (the "diode claims," requiring "at least one diode having a forward voltage drop that varies as a function of the temperature of the DRAM array" and corresponding signal), the Board formulated a *sua sponte* ground: Atkinson, Broadwater ***and Miller***. *Id*. Rather than grapple with the deficient way in which Miller had been used as supposed evidence of the finite number of alternatives, the Board reasoned that the Petition "relied" on Miller in the analysis of these claims, and decided to "therefore, treat Petitioner's analysis of Claims 2, 4, 10, 11, 14, 15, and 17 based upon Atkinson, Broadwater, and Miller from the statement as ***a separate ground*** of patentability," with Miller included as a third member of the alleged obviousness combination. Appx183 n.4. The Board rejected Polaris's argument in the preliminary response that there was no motivation to combine Miller—without, however, identifying any such alleged motivation. Thus, the Board instituted review on all challenged claims as follows:

References	Basis	Challenged Claims
Atkinson and Broadwater	§ 103(a)	1, 3, 5–9, 12, 13, and 16
Atkinson, Broadwater, and Miller	§ 103(a)	2, 4, 10, 11, 14, 15, and 17

Appx199.[2]

Polaris then filed its Response to the Petition, rebutting the instituted grounds. Appx210-279. Polaris challenged the Board's *sua sponte* ground based on "Atkinson, Broadwater, and Miller," because it, among other things, deprived Polaris of the right to file a preliminary response identifying reasons why that theory failed to meet the requirements of the statute. Appx236-245. Polaris also submitted argument, supported by direct and cross-examination testimony and documentary evidence, rebutting the two instituted grounds on the merits. Appx245-277. For example, Polaris showed that Atkinson, which is active only in a computer laptop's sleep mode, contains no teaching of "reducing the effects of thermal stress on the DRAM." Appx264. Polaris also demonstrated at least three objective indicia of nonobviousness: the long-felt need to alleviate DRAM's deleterious effects on energy efficiency and increased heat dissipation (Appx221); the unexpected result of alleviating both at the same time by adding to the DRAM's cost and complexity (Appx225-226); and the unexpected and synergistic result that the invention made possible of external synchronization of refresh rates with other signaling in SDRAM based on the actual temperature of the DRAM array (Appx227).

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[2] The Board's denial of institution on the other proposed grounds (*i.e.*, Grounds 3 and 4) is not before the Court. The Board instituted review on every challenged claim. *See SAS Institute Inc. v. Iancu*, 138 S. Ct. 1348 (2018). That determination was neither challenged before the Board nor appealed.

With its Reply, Kingston attached no evidence except for the transcript of the deposition of Polaris's expert. Appx280-309. Kingston raised, however, a host of new issues and arguments, that changed the issues and unpatentability rationales that had been raised in the Petition. For example, Kingston argued that the ordinary artisan would have been motivated to combine Atkinson and Broadwater to give Atkinson, a reference that operates only in sleep mode, "overheat protection" as a "safety measure," even though Atkinson has no teachings regarding overheating risk, has no external circuitry to monitor such risk, offers power dissipation in orders of magnitude well below the normal operation during the sleep mode, and shuts off all circuitry to take advantage of the low temperature in sleep mode to reduce the self-refresh rate for increased power efficiency. Appx285-286; Appx286-288; Appx295-296. Kingston also now argued that all "temperature sensors" were ***inherently*** "operable to produce a signal indicative of a temperature" that "may be provided to external circuitry" via a connection pin as the claims require—in other words, for the first time effectively reading the latter limitations out of the claims for the first time. Appx288-289.

Polaris asked the Board for a conference to request relief in light of the improper Reply arguments. Appx1421-1423. The Board denied Polaris's request for a conference, but allowed Polaris to file a short, non-argumentative list of new issues in the Reply. *Id*. In its rebuttal, Kingston did not argue that any of the new arguments

were actually in the petition, only that they were "supported" by the Petition. Appx318-322.

The Board then issued a Final Written Decision finding all challenged claims unpatentable. Appx43. The Board stated that none of the arguments or issues in Kingston's Reply was untimely, Appx17-18 n.6, and relied mainly on Kingston's arguments, without its own separate factual findings. *See, e.g.*, Appx13-17; Appx22-30; Appx32-37; Appx40; Appx42. The Board found that Atkinson taught or suggested the limitation of producing a signal indicative of a temperature of the DRAM array that may be provided to external circuitry over the connection pin. Appx14-15. The Board did not identify where this signal was produced in Atkinson, but concluded that it would have been obvious for an ordinary artisan to add it. Appx15-16. The Board found that Atkinson's teachings included "preventing [] overheating" and that it taught that it could overheat while in sleep mode. Appx22; Appx25. The Board refused to give any weight to Polaris's objective indicia, contending that the unexpected synergy with external synchronization was not entitled to weight because it was "not recite[d]" in the claim, and ignoring the other two indicia. Appx23.

With respect to the diode claims, the Board relied solely on its *sua sponte* ground including Miller to find unpatentability. Appx32; Appx42. The Board found that the motivation to add Miller's diode to Atkinson was "to enable the use of

Atkinson's DRAM in a 'cooling regime'," "to enable throttling of power to reduce heat," and to reduce "thermal stress in the DRAM." Appx35. But the Board's reason of "cooling regime" for combining Miller with Atkinson is not found in Miller although both Kingston and Kingston's expert suggested that it is. Appx69; Appx692-693. Miller does not discuss a "cooling regime" or any form of cooling. Appx966-972. Instead, it is Suzuki that mentions cooling control. Appx930. The Board's purported motivation to combine Miller and Atkinson and Broadwater thus relies in part on a motivation that is not found in any of the three references in the alleged combination, but a fourth reference the Board never added to the combination. Also, the Board ignored Polaris's evidence that adding Miller's diode to Atkinson's DRAM module would increase, not decrease, its continual power dissipation. *Compare* Appx33 *with* Appx 34-36.

IV. SUMMARY OF ARGUMENT

The Board's decision cancelling Polaris's patent claims was based on three critical errors, each one of which makes the decision unsustainable on appeal. It was based on an overbroad, implicit claim construction that negates the literal language of the claims. It was based on a new obviousness combination that was created by the Board in contravention of the Supreme Court's recent precedent. And it was based on factual determinations that cannot survive substantial evidence review.

First, the Board erred by implicitly nullifying the claim term "signal indicative of [a] temperature of the DRAM array," which the 057 patent requires to be capable of being output to an external circuitry so that it can ***cause*** the refresh rate from the external circuitry to change. According to the Board's obviousness determination, this internal signal that can be output to cause external changes to a refresh rate would be met by an ***internal*** refresh signal that cannot be output to indicate temperature. The Board's ***sub silentio*** construction thus nullifies the key distinction between the temperature signal and the phenomena it is meant to influence, as well as the key distinction between internal and external refresh control.

Second, the Board acted beyond its statutory authority when it instituted the IPR and cancelled Polaris's diode claims based on a ground that was not presented in the Petition. Here, the Board took critically deficient obvious-to-try evidence from a single-reference obviousness ground that was in the Petition and used it to craft a new three-reference obviousness combination that was not in the Petition. The Supreme Court's recent *SAS* decision laid to rest any doubt that the Board is allowed to institute an IPR or cancel claims on an unpetitioned ground and the Board's decision accordingly cannot stand. Moreover, even if considered on its merits, the PTAB's new ground cannot be sustained as it lacks substantial evidence; instead, it would render the primary reference, Atkinson, inoperable for its intended purpose.

Third, on the claims that do not specifically include diode limitations ("non-diode claims"), the Board erred by basing its unpatentability determination on findings unsupported by substantial evidence. The Board's purported motivation to combine Atkinson and Broadwater is based upon its determination that both Atkinson and Broadwater teach prevention against overheating. However, Atkinson has no such concern and in fact is directed exclusively to low-heat states, orders of magnitude cooler than ordinary—let alone overheated—operation. Further, the Board's decision lacks substantial evidence supporting the key portion of its obviousness analysis, namely, that Atkinson would have incorporated Broadwater's pin to maximize power saving. The Board also erred by not considering the impact of three objective indicia of nonobviousness.

Finally, the Board's decision must be set aside as a violation of the Appointments Clause of the United States Constitution because the PTAB judges, exercising significant authority pursuant to the laws of the United States, acted to terminate Polaris's patent rights even though they were never appointed by the President and never confirmed by the Senate.

V. ARGUMENT

A. Legal Standards

This Court reviews the Board's claim construction and ultimate determinations of obviousness *de novo* and the underlying factual findings for

substantial evidence. *Ariosa Diagnostics v. Verinata Health, Inc.*, 805 F.3d 1359, 1364 (Fed. Cir. 2015); *Lighting Ballast Control LLC v. Philips Elecs. N. Am. Corp.*, 744 F. 3d 1272, 1276-1277 (Fed. Cir. 2014) (en banc). Whether a ground the Board relied upon was new is a question of law subject to *de novo* review. *In re NuVasive, Inc.*, 841 F.3d 966, 970 (Fed. Cir. 2016). The "substantial evidence" standard "requir[es] a court to ask whether 'a reasonable mind might accept' a particular evidentiary record as 'adequate to support a conclusion.'" *Dickinson v. Zurko*, 527 U.S. 150, 162 (1999).

B. The Board Applied An Overbroad Interpretation Of "Signal Indicative Of The Temperature Of The DRAM Array" To Include Signals Not Outputtable To External Circuitry Via A Connection Pin

In its Final Written Decision, the PTAB improperly adopted an overbroad implicit construction of the recited "temperature sensor in thermal communication with the DRAM array, operable to produce a ***signal indicative of a temperature of the DRAM array***, and coupled to the at least one ***connection pin such that the signal may be provided to external circuitry***"[3] that the Board erroneously used to find this limitation disclosed in Atkinson. The plain language of the claim requires the "signal indicative of a temperature of the DRAM array" to be ***the same*** "signal that may be

[3] All emphases throughout Polaris's principal brief are added unless stated otherwise.

provided to external circuitry." But that is not the understanding the Board applied. The Board instead relied upon a refresh signal in prior art (Atkinson) as both a refresh signal and a temperature indicative signal, although they are claimed as separate signals, and the refresh signal in the prior art is not outputtable to external circuitry.

The Petition disavowed any need for claim construction. Appx62. Because Kingston offered no express constructions of the claims, Polaris had no burden to be the first to propose any constructions. The Final Written Decision likewise declined to adopt any express constructions. Appx7 ("We determine that it is not necessary to provide any express interpretation of the claim terms."). Nevertheless, as this Court has explained, "[d]espite no express construction of [the term] below, Board findings establishing the scope of the patented subject matter may fall within the ambit of claim construction. Because [Petitioner]'s challenge is directed to the Board's expression of its understanding of the scope of the claim term . . . , it is properly before us on appeal." *HTC Corp. v. Cellular Comm'ns Equipment, LLC*, 877 F.3d 1361, 1367 (Fed. Cir. 2017).

The Board's Final Written Decision found that Atkinson discloses a temperature sensor operable to produce a signal that may be provided to external

circuitry via a connection pin.[4] Appx14-15. But the Board nowhere identified a "signal indicative of a temperature" that is also ***the same*** signal that may be provided to external circuitry via a connection pin as claimed even though the claim language requires precisely that. Instead, the Board merely pointed to circuitry on Atkinson's DRAM module that generates a pulse that acts to refresh the DRAM. Appx15.

In identifying what it perceived as "[a]n example of a suitable temperature sensor," the Board relied upon Atkinson's "alternate embodiment" (Appx67) where a temperature sensor on the DRAM memory module itself provides a "voltage" to a voltage controlled oscillator ("VCO") "that represents the main memory temperature," causing the VCO to produce a "refresh signal" that refreshes the DRAM array. Appx14. But both the intrinsic and extrinsic evidence are contrary to the Board's broad and incorrect understanding of claim scope, which would make a refresh signal be the temperature-indicative signal that may be output to external circuitry. The claims, however, recite the "signal indicative of the temperature" that may be provided "to external circuitry," external to the DRAM array, and separately recite the refreshing of the DRAM array itself. Claim 13, for example, separately recites "a signal indicative of a temperature of the DRAM array" that may be

[4] Some of the claims' language relating to these limitations differs from one another, *e.g.*, *compare* Claim 1 *with* Claim 16, but the Final Written Decision addresses all seventeen claims in the same manner with respect to this limitation.

"provide[d] . . . to external circuitry" via a "connection pin;" and "refresh[ing] the DRAM array at a rate ***that varies in response to the signal***." Appx600-601. The specification also confirms that the claimed temperature-indicative signal that may be provided to external circuitry via a pin is not the same as the signal that refreshes the DRAM (*e.g.*, the signal 116 indicative of a temperature of the DRAM array 112 is not the same as the refresh signal 130 as shown in Fig. 3 above). Appx595; Appx599 (4:17-21, 4:30-32). The Final Written Decision itself also acknowledges the 057 patent's description of "***signal 116*** from temperature sensor 110 indicating a temperature sensed from DRAM array 112," and its separate description, in the same sentence, of "***refresh signal 130*** to refresh DRAM array 112 at a rate that varies in response to received ***temperature signal 116***," wherein the package containing the DRAM array "includes at least one connection pin 117 operable to provide the ***signal on line 116*** to external circuitry, such as the refresh unit 104" that "produces ***refresh signal 130***." Appx4-5 (quoting Appx599 at 4:30-32 and 4:49-53).

Moreover, the claim language requires that the temperature indicative signal may be outputted to an external circuitry. But Atkinson does not produce a temperature signal that can be provided via a pin to the external circuitry. As the Final Written Decision acknowledges, Kingston itself concedes that the embodiment relied upon in Atkinson "does not disclose providing the temperature signal to an external circuit," and merely contends it would have been obvious to provide such a

signal to such a circuit from the DRAM array. Appx15. But Polaris offered unrebutted expert testimony establishing that Atkinson has no active external circuitry to which to send such signals, and, moreover, could not generate a temperature indicative signal that could even be provided to the external circuitry via a connection pin without "wholesale modification of the control circuit" of Atkinson. Appx1099-1110 (¶ 55); Appx1103 (¶ 62); Appx1114 (¶ 88); Appx1278 (124:15-126:1). Therefore, Atkinson does not disclose this limitation. The Board ignored this evidence.

In a recent case, this Court reversed where the Board adopted an unreasonably broad construction of "signal" that ignored the requirement the claimed signal must meet. In *In re Hodges*, the Board found unpatentable claims reciting a "signal," where the written description made "clear . . . that the [claimed] signal must at least be capable of being compared to 'a predetermined limit,'" because the specification "explain[ed] that the sensor 'may transmit the signal to an indicator, such as a pressure gauge or alarm system, to provide a visual or audible indication of the operability of the drain valve,' and that a controller can 'compare[] the signal to a predetermined limit and generate[] a control signal based on this comparison'." 882 F.3d 1107, 1115 (Fed. Cir. 2018). This Court found that the Board adopted a "strained" and "unreasonably broad" interpretation of "signal" encompassing any "act, event, or the like that causes or incites some action," which "would encompass

virtually any . . . component within the valve drain that moves in response to the flow of fluid through the drain." *Id*. That interpretation was "unreasonable" because "the specification . . . state[d] that the sensor 'generates a signal,' which, in turn, can be transmitted to a pressure gauge to 'provide a visual … indication of the operability of the drain'"—"[i]n other words," the "'movement of' the . . . gauge's needle 'in response to the sensed pressure'" was not "itself" the recited "signal," according to the specification, but, rather, "the recited 'signal' causes the pressure gauge to provide a visual indication." *Id*. The prior art merely disclosed a movement of a piston, which, "[u]nder any reasonable construction of 'signal,' . . . cannot be compared to a predetermined limit, as described." *Id*.

Similarly, here, contrary to Kingston's suggestion that the claimed temperature signal may be the same as the refresh signal that pulses the DRAM in response to it, Appx303, the temperature signal that may be provided to the external circuitry cannot, in light of the intrinsic evidence, be interpreted to correspond to Atkinson's refresh pulse generator under any reasonable construction of that term.

The claimed "signal" may not be interpreted to encompass refresh signals or other signals that are not, without more, provided via a connection pin to indicate temperature. Because the Board purported to find these limitations in Atkinson and Atkinson merely generates refresh pulses that may not, without more, be provided via a connection pin to indicate temperature, and this error affects all cancelled

claims, its decision should be vacated. *See, e.g.*, *PPC Broadband, Inc. v. Corning Optical Communs. RF, LLC*, 815 F.3d 747, 756 (Fed. Cir. 2016) (vacating the Board's Final Decision because "the Board's construction is not reasonable in light of the specification"); *D'Agostino v. MasterCard Int'l, Inc.*, 844 F.3d 945, 947 (Fed. Cir. 2016) (vacating the Board's claim constructions "[b]ecause the Board's decisions rest on an unreasonable claim interpretation.").

C. The Board's Decision To Institute And Cancel Claims On A Ground Not Identified In The Petition Requires Reversal

The PTAB is not free to institute an IPR or invalidate claims on an unpetitioned ground. The Supreme Court has put to rest the notion that it could. *SAS*, 138 S. Ct. at 1348. And this Court has since recognized that such a deviation from the petition is not permissible under *SAS*. *Sirona Dental Sys. GmbH v. Institut Straumann AG*, No. 17-1341, 2018 U.S. App. LEXIS 16530 (Fed. Cir. 2018). That is what happened here. The Board instituted the IPR based on the three-legged obviousness combination of Atkinson, Broadwater, and Miller, against the diode claims, that was not in the petition, forcing Polaris to rebut that ground when Kingston had never made a *prima facie* showing. The Board's decision must be reversed.

1. The Board Cannot Institute An IPR Or Cancel Claims On An Unpetitioned Ground

The Board is not authorized to institute an IPR or cancel claims on unpetitioned grounds. In *SAS*, the Supreme Court laid to rest any notion to the contrary when discussing the PTAB's obligation in an IPR once instituted, to find on the patentability of all challenged claims. The Supreme Court explained that the statutory language:

> doesn't authorize the Director to start proceedings on his own initiative. Nor does it contemplate a petition that asks the Director to initiate whatever kind of inter partes review he might choose. Instead, the statute envisions that a petitioner will seek an inter partes review of a particular kind—one guided by a petition describing "each claim challenged" and "the grounds on which the challenge to each claim is based." §312(a)(3). From the outset, we see that Congress chose to structure a process in which it's the petitioner, not the Director, who gets to define the contours of the proceeding.

SAS, 138 S. Ct. at 1355. The Supreme Court further explained:

> ***More confirmation comes as we move to the point of institution.*** Here the statute says the Director must decide "whether to institute an inter partes review . . . pursuant to a petition." §314(b). ***The Director, we see, is given only the choice "whether" to institute an inter partes review. That language indicates a binary choice—either institute review or don't.*** And by using the term "pursuant to," ***Congress told the Director what he must say yes or no to: an inter partes review that proceeds "[i]n accordance with" or "in conformance to" the petition.*** OED, www.oed.com/view/Entry/155073.

Id. at 1355-56. The Supreme Court explained: "***Nothing*** suggests the Director enjoys a license to depart from the petition and institute a *different* inter partes review of his own design." *Id*. at 1356 (second emphasis in original).

> The rest of the statute confirms, too, that the petitioner's petition, not the Director's discretion, is supposed to guide the life of the litigation. For example, §316(a)(8) tells the Director to adopt regulations ensuring that, "after an inter partes review has been instituted," the patent owner will file "***a response to the petition***." Surely it would have made little sense for Congress to insist on a response *to the petition* if, in truth, the Director enjoyed the discretion to limit the claims under review. What's the point, after all, of answering claims that aren't in the proceeding?

Id (second emphasis in original). The Supreme Court thus expressly acknowledged that part of why the scope of the IPR must track the scope of the petition is ***because*** of the statutory right to respond to the petition itself. For these reasons, the PTAB is not free to "say yes" to a different ground than the one presented in the petition. Accordingly, this Court has explained, citing *SAS*, that "***It would thus not be proper for the Board to deviate from the grounds in the petition and raise its own obviousness theory*** . . . ." *Sirona*, 2018 U.S. App. LEXIS 16530, at *13.[5]

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[5] In *Sirona*, after acknowledging that *SAS* precluded deviating from the petition, this Court rejected appellant's argument "that the Board relied on theories that first appeared in the final written decision[.]" *Sirona*, 2018 U.S. App. LEXIS 16530, at *12. There the Board cancelled certain claims on an obviousness combination that ***was*** in the petition. *Id*. at *2-3. This Court concluded that "[t]he Board did not change theories simply because the petition did not use the exact words" that the Board used to describe the same reference in the same combination. *Id*. at *13. This Court also instructed the Board to consider on remand, under *SAS*, "whether it may consider combinations of references not argued by the petitioner in opposing [a] motion to amend claims, and, if so, what procedures consistent with the APA are required to do so," but only after first overruling the Board's decision on the same motion on other grounds. *Id*. at *16-17. Indeed, the Court only considered that additional obviousness combinations might be permissible only in the context of a motion to amend, making clear they are not permissible otherwise. This Court in *Sirona* has

The statute is consistent. An IPR can only be initiated when "a person who is not the owner of the patent" (35 U.S.C. § 311) files a detailed petition "identif[ying] with particularity," "the grounds on which the challenge to each claim is based, and the evidence that supports the grounds for the challenge to each claim." 35 U.S.C. § 312(a)(3). The patent owner has the "right to file a preliminary response to the petition . . . that sets forth reasons why no inter partes review should be instituted based upon the ***failure of the petition*** to meet any requirement of this chapter." 35 U.S.C. § 313. By regulation, the petition must identify "[t]he specific statutory grounds under 35 U.S.C. 102 or 103 on which the challenge to the claim is based ***and the patents or printed publications relied upon for each ground,***" and ***separately*** also identify "where each element of the claim is found in the prior art patents or printed publications relied upon." 37 C.F.R. §§ 42.104(b)(2), (5); *see also* §§ 42.108(a), (c). Instituting on unpetitioned grounds subverts ***both*** the requirement that the IPR only proceed on the basis of the petition, ***and*** the right of the patent owner to defeat institution on a showing a "***failure*** of the petition."

Further, instituting an IPR or cancelling claims on unpetitioned grounds shifts the burden to the patent owner to defeat the ground before making the petitioner present a *prima facie* case. *See In re Magnum Oil Tools Int'l, Ltd.*, 829 F.3d 1364,

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recognized the impact of *SAS*. Under the same reasoning in *Sirona*, the Board erred here.

1376 (Fed. Cir. 2016) ("We thus disagree with the PTO's position that the burden of production shifts to the patentee upon the Board's conclusion in an institution decision that 'there is a reasonable likelihood that the petitioner would prevail.'"); *id*. at 1380-81 (rejecting "the PTO's assertion that the Board did not err in making an obviousness argument on behalf of [the petitioner] based on the primary reference Lehr because this argument '***could have been included in a properly-drafted petition***[]'" and explaining that "[i]t is the petitioner that bears the burden of proof in IPRs.").

It follows that if the PTAB cannot ***institute*** on an unpetitioned ground, the PTAB also cannot ***cancel claims*** on an unpetitioned ground.[6] Even before *SAS*, this Court had recognized that the PTAB cannot cancel claims based on new grounds:

> We also are unpersuaded by [petitioner]'s attempts to cure the petition's deficiencies in its subsequent briefing to the Board and to us. . . . ***Here, Continental did not make out its obviousness case in its petition*** . . . . ***After [patent owner] pointed out the flaws of this position***, [petitioner]'s ensuing arguments to the Board and to us effectively abandoned its petition in favor of a new argument. . . . ***Rather than explaining how its original petition was correct, [petitioner]'s subsequent arguments amount to an entirely new theory of prima facie obviousness absent from the petition***. Shifting arguments in this fashion is foreclosed by statute, our precedent, and Board guidelines.

[6] The PTAB panel has properly refused to consider arguments if they were not raised in the petition. *See, e.g*., *Research In Motion Corp. v. MobileMedia Ideas LLC*, IPR2013-00016, Paper 19 at *3 (P.T.A.B. Apr. 2, 2013).

Wasica Fin. GmbH v. Cont'l Auto. Sys., Inc., 853 F.3d 1272, 1286 (Fed. Cir. 2017). As this Court has explained: "It is of the ***utmost importance*** that petitioners in the IPR proceedings adhere to the requirement that ***the initial petition*** identify 'with particularity' the 'evidence that supports the grounds for the challenge to each claim.'" *Intelligent Bio-Sys., Inc. v. Illumina Cambridge, Ltd.*, 821 F.3d 1359, 1369 (Fed. Cir. 2016). The PTAB cannot institute an IPR or cancel claims based on an unpetitioned ground.

2. The Board Impermissibly Instituted IPR And Cancelled The Diode Claims On An Unpetitioned Ground

Kingston identified ground one as obviousness based on Atkinson. In discussing that ground, Kingston relied upon Miller ***not*** as a combinable prior art reference but as evidence of the supposed knowledge of a person of ordinary skill in the art vis-à-vis what would have been obvious to try—citing Miller as supposed proof of the finite number of alternatives. Appx71. Relevant here, Kingston also identified a second ground of obviousness as based on Atkinson combined with Broadwater. In its discussion of that second ground, Kingston did not even mention Miller. When instituting the IPR, the Board did ***not*** institute the IPR against any claims based on the first ground, *i.e.*, Atkinson alone with its discussion of Miller. The Board ***did*** institute against certain claims based on the second ground, Atkinson combined with Broadwater. And then, the Board instituted against the ***diode*** claims based on a new ground that the Board created for the first time *sua sponte*—

"Atkinson, Broadwater, ***and Miller***"—and later cancelled those claims on that ground.

But Kingston never raised any obviousness combination based on Miller. Rather, the Board by its own admission created a "separate ground of patentability" for the diode claims, stating however that Kingston's mere reliance on Miller provided a basis to add such "separate ground." Appx183. The only reliance on Miller in the Petition (typos aside) is when it was described as an "example" of the finite options known to a skilled artisan. *See, e.g.*, Appx71 (discussing Atkinson); Appx91; Appx105 (discussing grounds not instituted): "[t]hose of ordinary skill at the time of the filing of the 057 Patent would know that one example of the finite alternate types of integrated circuits for detecting temperature was a diode having a forward voltage drop that varies as a function of temperature," and "[t]here is nothing inventive about using this known type of temperature sensor, and it would be obvious for a person of ordinary skill to have selected a diode." Appx71-72. Solely as part of its "finite alternate type" obvious-to-try argument about the Atkinson reference, Kingston pointed to, "[f]or example, Miller from 1974" as "describ[ing] a semiconductor diode 'temperature measuring apparatus' in which '[t]he temperature reading is made by measurement of the forward voltage drop across the diode.'" Appx71.

The Petition's "Proposed Grounds of Unpatentability" do not mention Miller. The "Summary of Grounds of Rejection" lists "Atkinson and Broadwater," but never mentions Miller. Appx60-61. The Petition's "Prior Art Offered for the Present Unpatentability Challenges" lists seven references, including Atkinson and Broadwater—but again, not Miller. Appx61-62. Similarly, Kingston's expert lists prior art and discusses its status as prior art, but does not mention Miller. Appx685-687; Appx1175 (117:1-25). The Petition's identification of "where the prior art teaches or suggests each portion of the claim, as well as . . . why a person of ordinary skill would be motivated to modify the base reference as outlined in the relevant obviousness combinations" identifies this ground repeatedly as "Atkinson in view of Broadwater" or "Atkinson and Broadwater"—and never mentions Miller. Appx62-63; Appx80; Appx81. The Institution Decision *sua sponte* converted Miller to a reference in a new combination. Appx183.

The Board expressly admitted that Kingston "omitted" the ground the Board instituted on, and confirmed that it instituted on that ground anyway. *See* Appx183 n.4 ("Although ***Miller is omitted from Petitioner's summary of asserted grounds***, it is nevertheless relied upon in Petitioner's analysis of claims 2, 4, 10, 11, 14, 15, and 17. *See, e.g.*, Pet. 20. We, therefore, treat Petitioner's analysis of claims 2, 4, 10, 11, 14, 15, and 17 based upon Atkinson, Broadwater, and Miller from the statement as a ***separate ground of unpatentability***."); Appx28-29 n.7. According to the Board,

"Petitioner's discussion of Miller within the content of the Petition ***as a way to bolster*** the Atkinson-Broadwater combination is tantamount to the Atkinson-Broadwater-Miller combination." Appx32. This is wrong: the Petition used Miller for a supposedly finite number of options, not in a combination; the Board used Miller to create a new combination.

The Board's argument that Kingston relied on Miller is irrelevant. The question is not whether Miller was discussed ***anywhere*** in the petition but whether there was a proposed ground in the petition expressly combining Miller with Atkinson and Broadwater. "Mere reliance on the same statutory basis and the same prior art references, alone, is insufficient to avoid making a new ground." *In re Leithem*, 661 F.3d 1316, 1319 (Fed. Cir. 2011).

Further proving that the Board changed grounds, when Polaris addressed Miller as an obvious-to-try argument in the preliminary response, the PTAB called that issue "moot" because of its decision to treat Miller as a combinable reference in its own right. But Kingston used Miller as part of a critically defective attempt to show obviousness to try. *See* Appx71 ("Those of ordinary skill at the time of the filing of the '057 Patent would know that ***one example*** of the ***finite alternate types*** of integrated circuits for detecting temperature was a diode having a forward voltage drop that varies as a function of temperature. Ex. 1005 at ¶ 53. ***For example, Miller*** from 1974 describes a semiconductor diode 'temperature measuring apparatus' in

which '[t]he temperature reading is made by measurement of the forward voltage drop across the diode.' Ex. 1015 at Abstract."). Polaris then refuted that argument in its preliminary response, as was proper. *See* Appx143 ("the number of alternative sensors usable to measure temperature is far from 'small or easily traversed,' as the caselaw requires. . . . The Petition does not provide . . . what would be the easiest proof that there is a small or easily traversed set of alternatives: a list of those alternatives."); Appx144 ("Miller is not part of any combination. No motivation is given to combine with Miller. It is therefore improper to rely on Miller for disclosure of a diode.").

The PTAB should have found that the obvious-to-try/finite-possibilities argument was legally defective. Instead, the Board ignored this defective argument, calling it "moot" in light of the decision to treat Miller as a combination reference in its own right. *See* Appx197 ("Patent Owner argues that Petitioner's reliance on 'finite alternate types of integrated circuits for detecting temperatures' is a misapplication of *KSR* because the number of available alternatives is 'far from 'small or easily traversed.'' . . . ***This argument is moot*** in light of Petitioner's alternative reliance upon Miller's diode to measure the temperature of Atkinson's DRAM. Pet. 20."). While the Board characterized this as "alternative reliance," there was no such reliance. There was only the one quote (*see* Appx71) in support of the finite possibilities argument. Thus, the Board brushed to one side the weakness of

the argument Kingston actually made in its petition, by declaring it "moot" in light of a different "alternative" ground that was not actually present in the petition—an "alternative" ground that was actually not Kingston's, but the Board's.[7]

Further confirming the *sua sponte* nature of the combination with Miller, the Board responded to Polaris's argument that there was no motivation to combine with Miller by stating: "Patent Owner also argues that Miller is not part of any combination and that no motivation is given by Petitioner to combine Atkinson with Miller. Prelim. Resp. 22. As discussed above, however, we interpret the ground of unpatentability as including Miller." Appx197-198. In other words, the Board did not grapple with the fact that the Petition itself did not contain a legally required element of the *prima facie* obviousness on the ground before the Board reinterpreted it *sua sponte*. Instead, the Board presumed its own conclusion that Miller was a combinable reference and, citing its own presumption, excused itself from needing an actual ***reason*** to combine Miller with Atkinson and Broadwater as a ground of institution.[8]

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[7] Trading a defective obvious-to-try argument for a three-reference obviousness combination changes the ***substance*** of the ground. *See In re NuVasive*, 841 F.3d at 972 ("In the related, non-IPR context, we have relied on the APA's requirements to find a 'new ground' where 'the thrust of the rejection' has changed, even when the new ground involved the same prior art as earlier asserted grounds of invalidity.").

[8] Even if it ***had*** grappled with the lack of motivation to combine, the Board may not add its own motivation to combine. *See Rambus Inc. v. Rea*, 731 F.3d 1248, 1256

Lastly, the Board tried to justify its decision to rely on a three-reference combination by adopting Kingston's argument that the Atkinson-Broadwater ground "builds off" the Atkinson ground that cited Miller. Appx32. This argument fails for at least two distinct reasons. ***First***, this argument does not address the distinction between a finite-alternatives argument and a combination. ***Second***, the Board was not free to presume that the arguments about Miller in the context of Atkinson ***alone*** (Ground 1) would work equally well in the context of Atkinson combined with Broadwater (Ground 2), particularly when Miller does not appear in Ground 2.

The Board's decision to institute and then cancel claims based on the three-reference combination including Miller was a legal error.

3. The Sua Sponte Ground Lacks Substantial Supporting Evidence

The Board's *sua sponte* theory still lacks substantial supporting evidence. Neither Atkinson nor Broadwater mentions forward-biased diodes. The fact that the claimed diode is a forward-biased diode, as opposed to just a diode or any other types of diodes, is significant. Kingston's expert acknowledged that there are many types of diodes and different types of diodes have different advantages and

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(Fed. Cir. 2013) ("The Board erred when it supplied its own reasons to combine . . . While the Board's findings may ultimately be correct, we will not affirm a Board rejection, like this one, which essentially provides a new motivation to combine the references.").

disadvantages. Appx1168 (89:19-20); Appx1169 (90:14-17). Polaris's expert testified that the claimed forward-biased diode specifically requires "a steady-state current to flow through a voltage drop" such that it "would be useful only during active mode" and "is appropriate … where significant power is already being dissipated due to its active state." Appx1118-1119 (¶ 100); Appx1119-1120 (¶ 102); Appx1121 (¶ 105). Because forward-biased diodes are "important structural limitation[s]," it would be an unusual case in which they could be added simply from the common knowledge of the ordinary artisan or any other such gap-filler theory. *Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1363 (Fed. Cir. 2016) ("[W]e conclude that while 'common sense' can be invoked, even potentially to supply a limitation missing from the prior art, it must still be supported by evidence and a reasoned explanation" in cases "where it is an important structural limitation that is not evidently and indisputably within the common knowledge of those skilled in the art …."). Because Kingston had not raised the purported combination of Atkinson, Broadwater, and Miller in the Petition, Kingston unsurprisingly offered no motivation to make that particular combination.

The Board offered two reasons for the purported combination, but neither is supported by substantial evidence and the Board ignored uncontradicted record evidence to the contrary. The Board argued that the ordinary artisan would have "substitut[ed] Miller's forward biased diode with *[sic]* Atkinson's thermistor" "to

enable the use of Atkinson's DRAM in a 'cooling regime' as well as 'to enable throttling of power to reduce heat as well as to monitor and track the memory temperature for diagnostic purposes,'" and to "predictably . . . reduc[e] thermal stress in the DRAM, upon being notified that the DRAM is overheating." Appx35. Not so.

First, as to the "cooling regime" motivation theory, the Board relied upon Kingston's Petition which represented that "'[o]ne of ordinary skill in the art would be motivated to send the signal indicative of memory temperature to an external connection pin, at least to enable its use in a cooling regime, ***such as the one set forth in Miller***.' Pet. 18." Appx34. But no "cooling regime" is described in Miller. Instead, despite Kingston's Petition (Appx69) and its expert's declaration (Appx692-693, ¶ 49) to the contrary, the passage Kingston relied upon, and the Board adopted, is from an entirely different reference, Suzuki, which was never discussed by the Board or Kingston. Appx140-141; Appx236 n.3; Appx951 (1:62-65). Therefore, the record before this Court does not identify what a combination of Atkinson-Broadwater-Miller-Suzuki would look like. Next, Kingston's argument about the "cooling regime" was not related to any diode claim, but to a limitation in the independent Claim 1 about the "signal that may be provided to external circuitry." Appx68-69.

Further, as will be explained in Section V(D) below, Atkinson has no teachings regarding overheating risk, thermal stress, or "monitor[ing]," has no active external circuitry to do such monitoring, and involved a "sleep" situation in which power dissipation was orders of magnitude below what it is during operation.

And even if any such teachings existed in Atkinson, the Board simply ignored Polaris's uncontradicted evidence that "the continuous current drain required to sense the temperature through a forward biased diode would ***increase*** the steady state power during this sleep mode compared to the current circuit in Atkinson," which would lead to the opposite of what Atkinson desired ***and*** render Atkinson inoperable for its intended purpose, which was to reduce energy consumption during system suspend mode—exactly the reason why Atkinson pointedly left diodes off its list of suitable temperature sensors for its sleep mode circuit. Appx272-273; Appx1108-1109 (¶ 79); Appx1114-1115 (¶ 91); Appx1119-1120 (¶¶ 101-102). No substantial evidence, therefore, supports the Board's determination on a ground not found in the Petition. *See PersonalWeb Techs. LLC v. Apple*, Inc., 848 F.3d 987, 994 (Fed. Cir. 2017) (concluding that the Board provided an inadequate analysis to provide meaningful appellate review); *In re Nuvasive*, 842 F.3d at 1384–85 (remanding for failure to articulate a motivation to combine).

D. The Board Improperly Found The Non-Diode Claims Obvious Over Atkinson And Broadwater

For the non-diode claims (*i.e.*, Claims 1, 3, 5–9, 12, 13, and 16), the Board also erred in determining that the claims are obvious over the combination of Atkinson and Broadwater. The Board based its determination on finding two motivations to combine: to prevent "thermal stress" from "overheating," and to "maximize power saving." Appx15-16; Appx22-23; Appx25-27. The first is predicated on a finding that Atkinson is vulnerable to overheating and teaches its prevention, which was first raised in the Reply, and is unsupported by any substantial evidence. The second ignores Atkinson's non-operation application and lack of active external circuitry. Separately, the Board failed to address at least two of Polaris's objective indicia of nonobviousness, including the invention's satisfaction of a long-felt need and achievement of unexpected results, and as for the one indicium it did consider, the Board rejected it, stating that it is not recited in the claims. These rulings should be reversed.

1. No Substantial Evidence Supports The Board's Determination That Atkinson Teaches Overheating Prevention

The Board's determination of motivation to combine is based upon its determination that both Atkinson and Broadwater teach "optimizing the performance of integrated circuits ***by preventing the overheating thereof*** thereby enhancing reliability, temperature, and power consumption of integrated circuits."

Appx22 (finding that "so long as Atkinson's DRAM is subject to disrupted operation due to possible overheating (in the sleeping mode or wake state) and includes a temperature sensor that outputs the sensed temperature of the DRAM, its proposed combination with Broadwater would be proper because Broadwater's thermal stress reduction technique would help cool down the chip"); Appx26 (finding that "the laptop disclosed in Atkinson is vulnerable to overheating even in sleep mode"); *see also* Appx16; Appx21; Appx25 (similar). No substantial evidence supports this determination. Any chip in the world could overheat if something external were to overheat it. However, Atkinson's teachings are exclusively directed to extremely low-heat states, orders of magnitude cooler than ordinary—let alone overheated—operation. Appx1098-1099 (¶ 54).

As described above in Sections III(C) and V(C)(3), every single embodiment in Atkinson is exclusively devoted to saving power in "lower power mode" with the system asleep, by reducing the rate of DRAM refresh according to the expected or measured reduction in temperature during such sleep mode. Appx 1098 (¶ 51); Appx895 (13:11-18) ("During low power modes, the present invention advantageously refreshes memory at a slower rate than during normal operation."); Appx900 (23:40-48, 23:65-67); Appx1098 (¶ 52); Appx1111-1112 (¶ 83). The Board never identified anything in Atkinson even suggesting that Atkinson had the slightest concern with overheating. Its finding to the contrary appears to be implicitly

based on unwritten knowledge of the ordinary artisan. But the record establishes, in unrebutted expert testimony, that the power dissipation on the DRAM module when Atkinson's invention is operating is at least 100 times, and possibly 1,000 times—two to three orders of magnitude ***lower***—than during normal system operation. Appx1109-1110 (¶¶ 80-81).

But even if there were an overheating concern in Atkinson, it could not possibly motivate the ordinary artisan to make the invention, because, as Polaris explained and the Board ignored, in situations of increasing heat the claimed invention ***increases***, rather than ***decreases***, the temperature of the memory array, thereby only exacerbating any concern about "overheating." As previously explained, the higher the temperature of a DRAM array rises, the higher the refresh rate generally must be to prevent data loss, and vice versa. Appx598 (1:51-55, 1:66-2:2, 2:26-37, 2:63-67); Appx599 (4:18-22, 4:30-37, 4:48-53); Appx600 (5:37-48, 5:60-6:7). Atkinson takes advantage of this very same property in its specific context, which is restricted to the dramatically lower power dissipation of suspend or sleep mode with all external circuitry off, and which takes advantage of the dramatically lower temperatures of sleep mode to reduce the self-refresh rate for increased overall power efficiency. Appx219; Appx1111-1113 (¶¶ 83-84); Appx1114-1115 (¶¶ 91). The 057 patent, however, goes well beyond Atkinson, because the inventor realized that the invention could increase both efficiency and

bandwidth by permitting a relatively lower refresh rate overall ***during operation***. Appx223; Appx1090-1091 (¶ 39); Appx1092-1094 (¶¶ 41-42). Thus, the 057 patent provides an external refresh unit with a signal indicative of the actual temperature of the DRAM array in order to send a refresh signal increasing the refresh rate based on that signal. Appx224-225; Appx1091 (¶ 40); Appx1092-1094 (¶¶ 41-42). Atkinson, limited only to power efficiency, did not come to the same insight as the 057 patent inventor. Appx156; Appx218-219; Appx1105 (¶ 67).

Having no other supporting evidence at their disposal, Kingston and the Board pointed "chiefly" (Appx21) to a comment Polaris's expert, Professor Bernstein, made in deposition about devices "blowing up" *[sic]*. But this snippet of testimony not only has nothing to do with preserving DRAM data by increasing the refresh rate, it has nothing to do with Atkinson overheating—as Professor Bernstein himself emphasized in that same cross-examination response. Professor Bernstein commented that both Atkinson and Broadwater were, in some sense, "concerned with power and reliability," and, in so doing, mentioned that ***Broadwater—not*** Atkinson—was "concerned with the power for its potential operation. We don't want the device to blow up . . . ." Appx1257 (40:5-18, 38:24-39:14). That has nothing to do with Atkinson overheating or with controlling DRAM refresh rate proportional to temperature.

Professor Bernstein's other cited testimony in fact contradicts the Board's theory. Asked a hypothetical question involving a "fire" potentially breaking out in a "large data center" when the air conditioning in a "server room" failed and "it got very, very hot," Professor Bernstein testified that in such "data centers," there could be systems in which, "rather than start a fire, they would be – shutdown everything, which would include data loss." *Id.*, Appx1282 (138:17-141:12). This hypothetical, of course, has no relationship to Atkinson's DRAM module in its sleeping laptop—as Professor Bernstein pointed out, observing immediately afterward that "at the level we're talking about, on the board level, I've honestly never heard of such a thing where there's a sensor that's concerned about it being burned up on the device level." Appx1282 (141:13-16); Appx1108 (¶ 78). Such mechanisms, Professor Bernstein testified, existed "at the big system level," but he had "never heard of them implementing such a system like Broadwater . . . at the board level," let alone "at the chip level" as the hypothetical proposed. Appx1282 (141:13-16); Appx1282-1283 (141:23-142:6); Appx1283 (142:7-14). Rather than support the Board's finding, Professor Bernstein's testimony refutes it.

Like the petitioner in *Elbit Systems of America, LLC v. Thales Visionix, Inc.*, Kingston and the Board "fail[] to present any evidence supporting this contention beyond attorney argument, and 'attorney argument is not evidence' and cannot rebut other admitted evidence. In contrast, [the patent owner]'s expert testified [to the

opposite effect]." 881 F.3d 1354, 1359 (Fed. Cir. 2018); *accord, e.g.*, *ICON Health & Fitness, Inc. v. Strava, Inc.*, 849 F.3d 1034, 1043 (Fed. Cir. 2017) ("Attorney argument is not evidence. . . . [T]he PTAB's adoption of [requester]'s [briefing] [did not] transform [requester]'s attorney argument into factual findings or supply the requisite explanation that must accompany such findings. . . . [T]he PTAB must make the necessary findings and have an adequate evidentiary basis for its findings."); *Wasica*, 853 F.3d at 1284.

2. No Substantial Evidence Supports The Determination That Atkinson Would Have Added Broadwater's Pin To Maximize Power Saving

As noted above, the Board rested its obviousness determination on finding a motivation to combine from "the dual benefit of maximizing power saving during self-refresh timing sequence, as well as reducing thermal stress on the DRAM." Appx25; *see also* Appx16. Even aside from the lack of substantial evidence discussed above, there is also no substantial evidence that Broadwater's pin would "maximiz[e] power saving." Appx1111-1112 (¶ 83).

The Board asserted without citing evidence or conducting its own analysis: "We are persuaded that a person having ordinary skill in the art would have found it obvious to combine the teachings of Atkinson and Broadwater because we agree that transmitting the sensed temperature of the DRAM to an external circuit via an external pin would have been recognized by a person having ordinary skill in the art

as resulting in a more efficient system that maximizes power saving by reducing thermal stress on the packaged semiconductor chip." Appx16. But it is undisputed that Atkinson operated exclusively in "low power mode," with all external circuitry asleep and the system clock off. Appx 1098 (¶ 51); Appx891 (6:5-11); Appx895 (14:10-31); Appx900 (23:43-46, 24:22-28, 24:40-44); Appx1098 (¶ 52); Appx1106 (¶¶ 71, 73). In such a situation, there is no external circuitry awake to ***use*** any information sent over a pin to save power. Appx264; Appx1111-1112 (¶ 83); Appx1114 (¶ 89).

Moreover, the Board ignored the other teachings in the combination discouraging or teaching away from making the invention. In addition to the fact that the invention exacerbates rather than reduces any overheating concerns, the Board acknowledged the point raised by Polaris that Atkinson's cited embodiment "was designed to be self-contained to include the temperature sensing refresh generator within main memory 906," Appx19, so that it could "conveniently be incorporated into any computer system by substituting memory modules." Appx900 (24:22-27); Appx1102-1103 (¶ 61); Appx1108-1109 (¶ 79). But the Board then proceeded to ignore this teaching, and argued that it is "not commensurate in scope with the claim language," and that Polaris did not "provid[e] any basis in the claims to support the argument that Atkinson's system cannot be modified as proposed to add an external connection pin to complement the refresh process." Appx22-23. The

Board stated no basis that discouraging teachings or teaching away may be ignored because it is not recited in "the claim language" of the claim challenged with obviousness; instead, the law on teaching away focuses on whether one of ordinary skill would be discouraged from modifying Atkinson's system. *DePuy Spine, Inc. v. Medtronic Sofamor Danek, Inc.*, 567 F.3d 1314, 1327 (Fed. Cir. 2009) ("A reference may be said to teach away when a person of ordinary skill, upon reading the reference, would be discouraged from following the path set out in the reference, or would be led in a direction divergent from the path that was taken by the applicant.").

E. The Board Improperly Ignored The Objective Indicia Of Nonobviousness Relevant to All Cancelled Claims

The Board also failed to address substantively any of the objective indicia of nonobviousness that Polaris identified, including the long-felt need to improve efficiency and reduce performance impacts of DRAM refresh; the unexpected result of the patent's success in achieving both simultaneously (*e.g.*, increasing overall efficiency through saving power and increasing bandwidth by permitting a relatively lower refresh rate overall during operation under moderate temperatures); and the unexpected synergy of the 057 patent's external control over refresh rate with the emerging paradigm shift to "deterministic" system synchronization of the refresh in SDRAM.

Polaris presented these indicia of nonobviousness in detailed descriptions. Appx222 ("The DRAM refresh process creates significant disadvantages, the

alleviation of which has been a long-felt need in the computer industry."); Appx263 ("The most unexpected benefit of the invention claimed in the '057 Patent is that it facilitates efficient, deterministic control of the DRAM in sync with the rest of the activity in the system."); Appx227 ("The invention provides still more unexpected results."); *see also* Appx218; Appx221; Appx226; Appx263; Appx385-387; Appx1087 (¶ 34); Appx1088 (¶ 35); Appx1090-1091 (¶ 39); Appx1095-1096 (¶ 45); Appx1110-1111 (¶ 82); Appx1259 (48:18-49:19); Appx1288-1289 (165:12-166:1).

But the Board only addressed, though not substantively, one of those three objective indicia of nonobviousness—*i.e.*, the unexpected benefit and result of using external control to facilitate efficient, deterministic control of the DRAM in sync with the rest of the activity in the system. Appx23. The Board dismissed it instead of weighing it against other evidence, stating that the claims do not recite this objective indicium. *Id*. That is not the law. In *Rambus*, 731 F.3d at 1256-57, this Court stated, "[t]he Board erred when it found that [Patent Owner's] objective evidence of nonobviousness lacked a nexus … [and] was not commensurate with the scope of the claims because the claims 'do not recite a specific clock speed and therefore embrace slow memory devices.' … Such a strict requirement was improper." It is also well settled that "[t]he invention as a whole embraces the structure, its properties, and the problem it solves." *In re Wright*, 848 F.2d 1216, 1218-20 (Fed. Cir. 1988); *In re Magnum*, 829 F.3d at 1375-77. For nonobviousness

purposes, disclosed "use[s]" and "unexpected propert[ies]" of an invention "cannot be ignored. The issue here is not whether a claim ***recites*** a new use, but whether the subject matter of the claim ***possesses*** an unexpected use. That unexpected property is relevant, and thus the declarations describing it should have been considered by the Board." *In re Sullivan*, 498 F.3d 1345, 1352-53 (Fed. Cir. 2007). Nor is it relevant that the properties reflected in and affecting objective indicia are inherent in the invention or that the invention's components are known or feasibly combined by the ordinary artisan. "What is important regarding properties that may be inherent, but unknown, is whether they are unexpected." *Honeywell Int'l Inc. v. Mexichem Amanco Holding S.A. de C.V.*, 865 F.3d 1348, 1355 (Fed. Cir. 2017).

The Board ignored the other two indicia of non-obviousness. But this Court has consistently required the Board to consider the objective indicia of nonobviousness before reaching its conclusion. *PPC Broadband, Inc. v. Iancu*, No. 2017-1362, -1363, and -1364, 2018 U.S. App. LEXIS 18297, at *29-30 (Fed. Cir. 2018) (finding "the Board simply ignored [the Court's] directive to give due weight to these indicia of non-obviousness in its obviousness analysis and the evidence that prompted it" and instructing the Board to "consider PPC's objective indicia evidence anew and consider this evidence" on remand); *Plantronics, Inc. v. Aliph, Inc.*, 724 F.3d 1343, 1355 (Fed. Cir. 2013). Such evidence "cannot be overlooked" and can "serve to resist the temptation to read into the prior art the teachings of the invention

in issue." *Id*. (quoting *In re Cyclobenzaprine Hydrochloride Extended–Release Capsule Patent Litig*., 676 F.3d 1063, 1076 (Fed. Cir. 2012)). Yet, that is exactly what the Board did here, and this is another basis, in addition to the above independent reasons, why the Board's obviousness determination should be reversed.

F. The Board Members Could Not Constitutionally Issue A Final Agency Decision Eliminating Patent Rights Without Having Been Appointed By The President And Confirmed By The Senate

An independent ground on which this Court should set aside the Board's decision is that it exceeded the powers permitted to the Board under the Constitution's Appointments Clause, Art. I, § 2, cl. 2. The PTAB judges, on behalf of the USPTO and the federal government, entered a final decision that Polaris's issued claims are unpatentable and subject to mandatory cancellation—without meaningful Executive Branch supervision or review. 35 U.S.C. §§ 311(a), 316(c), 318(a)-(b). The Appointments Clause requires, however, that only "principal Officers" of the United States appointed by the President and confirmed by the Senate may "exercis[e]" such "significant authority pursuant to the laws of the United States." *Buckley v. Valeo*, 424 U.S. 1, 126 (1976) (per curiam). All administrative patent judges ("APJs") before 1975 were so nominated and confirmed, *id*. at n.22, and would have been empowered to make such decisions for purposes of the Clause. The PTAB judges who decided this case were not. In the

absence of such appointment and of meaningful supervision and review, these PTAB judges are not empowered to render final written decisions eliminating patent owners' rights.

The Court should consider this question on appeal because the defect in the appointment of PTAB judges goes to the validity of PTAB's proceeding and is dispositive. *See Freytag v. Commissioner*, 501 U.S. 868, 878-79 (1991) ("The alleged defect in the appointment of the Special Trial Judge goes to the validity of the Tax Court proceeding that is the basis for this litigation. . . . We conclude that this is one of those rare cases in which we should exercise our discretion to hear petitioners' challenge to the constitutional authority of the Special Trial Judge.").

1. PTAB Judges Who Decide IPRs Are Incontestably "Officers" Of The United States Under The Constitution's Appointments Clause

As the federal government recently summarized before the Supreme Court:

> The Appointments Clause sets out the exclusive method for appointment of all [subordinate] Executive Branch officers whose appointments are not otherwise provided for in the Constitution. "[P]rincipal Officer[s]" are appointed by the President, by and with the advice and consent of the Senate; the same method applies to "inferior Officers," except where their appointments have instead been vested by law "in the President alone, in the Courts of Law, or in the Heads of Departments." U.S. Const. Art. II, § 2, Cls. 1, 2 . . . .

Brief for Respondent SEC at 11, *Lucia v. SEC*, 868 F.3d 1021 (D.C. Cir. 2017), *cert. granted*, 138 S. Ct. 736 (2018), *rev'd*, No. 17-130, 2018 U.S. LEXIS 3836, 585 U.S. ___ (June 21, 2018). Under the Appointments Clause, all constitutional Officers are

either "principal" or "inferior." *Buckley*, 424 U.S. at 125 (citing *United States v. Germaine*, 99 U.S. 508, 509-510 (1879)).

Anyone who occupies a "'continuing' position established by law" and "exercis[es] significant authority pursuant to the laws of the United States" is an "Officer" under the Appointments Clause, and not merely an employee. *Lucia*, 2018 U.S. LEXIS 3836, at *12 (internal citations omitted). In *Freytag*, for example, the Supreme Court held that special trial judges of the U.S. Tax Court were constitutional "Officers" subject to the requirements for such officers under the Appointments Clause, and not mere employees of the Executive Branch. 501 U.S. at 881. Even though the Tax Court special judges "lack[ed] authority to enter a final decision" on behalf of the government, they nevertheless were Officers because they had "significan[t] . . . duties and discretion," occupied an office "'established by Law'" with "duties, salary, and means of appointment . . . specified by statute," "t[ook] testimony, conduct[ed] trials, rule[d] on the admissibility of evidence, and ha[d] the power to enforce compliance with discovery orders" in their adjudications. *Id*. Moreover, applying the factors set forth in *Freytag*, the Supreme Court just last month, in *Lucia,* held that administrative law judges who render decisions in SEC adjudications are Officers of the United States subject to the requirements of the Appointments Clause, not mere employees. *Lucia*, 2018 U.S. LEXIS 3836, at *6.

Applying the criteria set forth in *Freytag* and *Lucia* renders it beyond reasonable dispute that PTAB judges who decide IPRs are "Officers" under the Clause. First, they occupy non-temporary offices established by law. 35 U.S.C § 6 (2012). They have duties, salaries, and means of appointment specified by statute. *Id*.; 35 U.S.C § 3(b)(6) (2012). Second, they exercise significant authority pursuant to the laws of the United States. 35 U.S.C § 6 (2012). Just like the officers in *Freytag* and *Lucia*, they take testimony, conduct trials, apply federal rules of evidence and rule on admissibility of evidence, and conduct discovery. *Compare Lucia*, 2018 U.S. LEXIS 3836, at *16, *with Merck & Cie v. Gnosis S.P.A.*, 820 F.3d 432, 435 (Fed. Cir. 2016). They issue final decisions on the agency's behalf that extinguish the rights of patent owners. *Compare Lucia*, 2018 U.S. LEXIS 3836, at *17, *with Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2137, 2143 (2016). Indeed, PTAB judges are even more independent than Tax Court judges or SEC ALJs, because their decisions are always final and not reviewable even by the USPTO's Director. Even more, the Board's IPR decisions enjoy an exceedingly deferential standard of review: the only review that parties may obtain as of right is an appeal to this Court, where this court affords the Board broad discretion; does not reweigh evidence; and upholds all factual findings supported by substantial evidence in the record.

2. Because PTAB Judges Issue Final IPR Decisions Eliminating Patent Rights, They Must Be "Principal Officers"

Given that PTAB judges are constitutional Officers, under the Appointments Clause, they must be either inferior Officers or principal Officers. As explained below, they are the latter. PTAB judges deciding IPRs exercise significant independent discretion, are not removable from the competitive service except for cause, and issue final decisions conclusive upon patent rights, not subject to change by any superior officer in the agency or the Executive Branch, and subject to only limited and deferential review. Collectively, these characteristics demonstrate that PTAB judges act as principal Officers under the Clause.

In particular, PTAB judges are not subject to peremptory removal, but enjoy the same good-cause removal protections as any member of the competitive service. 5 U.S.C. §§ 7521, 432.102(b)(6), 2102(a); 35 U.S.C. § 3(c). They enjoy broad powers to order discovery. They make final decisions on the agency's behalf, subject to minimal or no oversight in these decisions. And their office is not limited in tenure or temporary.[9] 35 U.S.C § 6 (2012).

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[9] *Compare with Free Enter. Fund v. PCAOB*, 561 U.S. 477, 486, 510 (2010) (finding members of Public Company Accounting Oversight Board to be inferior officers because statute "places the Board under the SEC's oversight," and SEC may fire Board members and overrule Board's sanction orders and rules at will).

In a precedential decision that the Office of Legal Counsel adopted and characterized in 1978 as "generally accepted," 2 Op. O.L.C. 58, 58-59 (1978), the Court of Claims held that whether an officer is an "inferior" Officer under the Clause depends not on whether he is "petty or unimportant," but whether he is "subordinate or inferior to those officers in whom respectively the power of appointment may be vested—the President, the courts of law, and the heads of departments," in other words, "one who is bound to obey another." *Collins v. United States*, 14 Ct. Cl. 568, 574 (1878). PTAB judges are not such officers because no other agency officer has the power to review or overrule the Board's IPR decisions. By statute, their decisions on behalf of the agency are final. 35 U.S.C. §§ 141(a), 314(d), 319.

The courts of appeals that have addressed the question of whether Officers are principal or inferior in similar circumstances have found Officers with similar authority to that of PTAB judges to be principal Officers. *See Ass'n of Am. R.R. v. United States DOT*, 821 F.3d 19, 39 (D.C. Cir. 2016) (holding that railroad passenger rate arbitrators are "principal Officers" because the act "doesn't provide any procedure by which the arbitrator's decision is reviewable by the [Surface Transportation Board]. . . . The result? A final agency action . . . . Without providing for the arbitrator's direction or supervision by principal officers, [the relevant statute] impermissibly vests power to appoint an arbitrator in the STB."), *reh'g*

denied mem. (D.C. Cir. 2016) (*per curiam*); *Intercollegiate Broad. Sys., Inc. v. Copyright Royalty Board*, 684 F.3d 1332, 1336-40 (D.C. Cir. 2012) (holding that Copyright Royalty Board members who exercised significant discretion and issued final agency decisions were "principal Officers" for constitutional purposes). Under the standards applied in those appellate decisions, PTAB judges who decide IPRs must act as principal Officers.

No one in the agency directly supervises PTAB judges' decisions. No member of the agency can order rehearing of their decisions: on the contrary, the power to grant rehearing of the Board's decisions in IPRs rests with the Board itself. 37 C.F.R. § 42.71(d)(2). PTAB judges, in order to render final IPR decisions eliminating patent rights, must be principal Officers.

Indeed, until 1975 all USPTO administrative patent judges were nominated by the President and confirmed by the Senate. 35 U.S.C. § 3 (1952). The Patent Act was then amended to eliminate such nomination and confirmation. 35 U.S.C. § 3 (1975). Today, all PTAB judges are "appointed by the Secretary of Commerce in, consultation with the Director" of the USPTO. 35 U.S.C. § 6(a) (2008).

The current means of appointment of APJs would satisfy the Appointments Clause if APJs were inferior Officers. But as discussed above, APJs are principal Officers, and therefore, they must be nominated by the President and confirmed by the Senate.

3. The Final Written Decision Must Be Set Aside On The Basis Of The Board Members' Improper Appointment

Given that the Board judges are not constitutionally appointed, this Court must decide on the appropriate remedy. In *Ryder v. United States*, the Supreme Court held that a claimant "is entitled to a decision on the merits" as the effect of a violation is not prospective only, but controls the hearing and trial: the Constitution requires a new proceeding in front of a constitutionally appointed panel, with no validity given to the prior acts. 515 U.S. 177, 182-88 (1995) Furthermore, Section 706 of the Administrative Procedure Act, which applies to IPRs, provides that upon a finding of constitutional violation, the reviewing court "shall . . . set aside agency action, findings, and conclusions found to be . . . contrary to constitutional right [or] power." 5 U.S.C. § 706(2)(B). The Supreme Court held in *Lucia* that the appropriate remedy for an Appointments Clause violation is a "new 'hearing before a properly appointed' official" ***other*** than the officials who already "heard [the] case and issued [the] decision" appealed from. *Lucia*, 2018 U.S. LEXIS 3836, at *21. Because the manner of the PTAB judges' appointment violates the Appointments Clause, the Final Written Decision in this case, if not reversed or vacated on nonconstitutional grounds, must be set aside and this case must be re-heard, if at all, before members of the Board who are constitutionally appointed.

VI. CONCLUSION AND STATEMENT OF RELIEF SOUGHT

For the foregoing reasons, the Court should reverse the Board's determination that Claims 1-17 of the 057 patent are unpatentable under 35 U.S.C. § 103.

Dated: July 10, 2018

Respectfully submitted:

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FORM 30. Certificate of Service Form 30

UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

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UNITED STATES COURT OF APPEALS FOR THE FEDERAL CIRCUIT

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(Signature of Attorney)

Matthew D. Powers

(Name of Attorney)

Appellant

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ADDENDUM

INDEX

Trials@uspto.gov
571-272-7822

Paper 33
Entered: January 29, 2018

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KINGSTON TECHNOLOGY COMPANY, INC.,
Petitioner,

v.

POLARIS INNOVATIONS LTD.,
Patent Owner.

Case IPR2016-01621
Patent 6,438,057 B2

Before SALLY C. MEDLEY, JEAN R. HOMERE, and KEN B. BARRETT, *Administrative Patent Judges*.

HOMERE, *Administrative Patent Judge*.

FINAL WRITTEN DECISION
Inter Partes Review
35 U.S.C. § 318(a) and 37 C.F.R. § 42.73

I. INTRODUCTION

In this *inter partes* review, instituted pursuant to 35 U.S.C. § 314, Kingston Technology Company, Inc. ("Petitioner") challenges claims 1–17 ("the challenged claims") of U.S. Patent No. 6,438,057 B1 (Ex. 1001, "the '057 patent"), owned by Polaris Innovations Ltd. ("Patent Owner").[1] We have jurisdiction under 35 U.S.C. § 6. This Final Written Decision is entered pursuant to 35 U.S.C. § 318(a) and 37 C.F.R. § 42.73. For the reasons discussed below, Petitioner has shown by a preponderance of the evidence that the challenged claims are unpatentable.

A. Procedural History

Petitioner filed a Petition requesting an *inter partes* review of claims 1–17 of the '057 patent. Paper 2 ("Pet."). Patent Owner filed a Preliminary Response. Paper 7 ("Prelim. Resp."). On February 15, 2017, we instituted *inter partes* review of claims 1, 3, 5–9, 12, 13, and 16 of the '057 patent under 35 U.S.C. § 103(a) as being unpatentable over the combination of Atkinson,[2] and Broadwater.[3] Paper 8 ("Inst. Dec."), 17. Further, we instituted *inter partes* review of claims 2, 4, 10, 11, 14, 15, and 17 of the '057 patent under 35 U.S.C. § 103(a) as being unpatentable over the combination of Atkinson, Broadwater, and Miller.[4] *Id.* at 20.

Thereafter, Patent Owner filed a Patent Owner Response (Paper 18, "PO Resp."), to which Petitioner filed a Reply (Paper 21, "Reply").

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[1] Patent Owner identifies Polaris Innovations Ltd., Wi-LAN Inc., and Quarterhill Inc. as real parties-in-interest. Paper 4, 2; Paper 20, 2.
[2] U.S. Patent No. 6,134,167, issued Oct. 17, 2000 (Ex. 1010) ("Atkinson").
[3] U.S. Patent No. 4,970,497, issued Nov. 13, 1990 (Ex. 1006) ("Broadwater").
[4] U.S. Patent No. 3,812,717, issued May 28, 1974 (Ex. 1015) ("Miller").

Pursuant to an Order (Paper 22), Patent Owner filed a listing of alleged statements and evidence in connection with Petitioner's Reply that Patent Owner considered to be beyond the proper scope of a reply. Paper 23. Petitioner filed a response to Patent Owner's listing. Paper 24.

We held a consolidated hearing on November 14, 2017, for this case and related Cases IPR2016-01622 and IPR2016-01623, and a transcript of the hearing is included in the record. Paper 32 ("Tr.").

B. Related Proceedings

The parties state that the '057 patent is the subject of a pending lawsuit in the Central District of California Southern Division that includes assertions against Petitioner. Pet. 2; Paper 4 (Patent Owner's Mandatory Notice), 1; Ex. 1002.

C. The '057 patent (Ex. 1001)

The '057 patent is directed to a method and system for refreshing the contents of a dynamic random access memory (DRAM) array. Ex. 1001, 1:5–7. In particular, the temperature of the DRAM array is utilized to adjust a refresh rate at which the contents of the DRAM array are updated. *Id.* at 1:7–10. Figure 3 of the '057 patent is reproduced below:

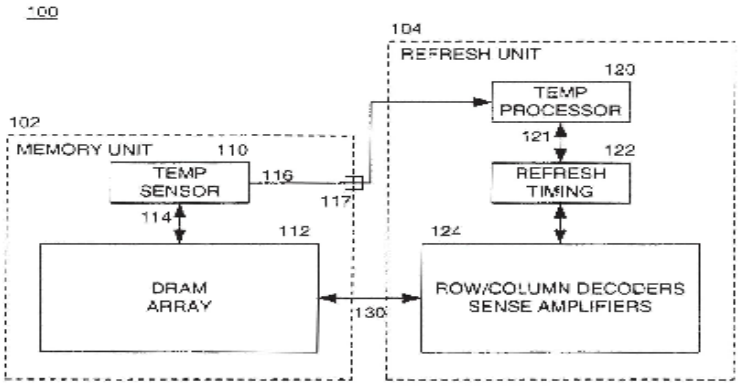

FIG. 3

Figure 3 illustrates system 100 for storing data in DRAM array 112. *Id.* at 4:11–12. In particular, Figure 3 depicts memory unit 102 containing temperature sensor 110 coupled to DRAM array 112, wherein memory unit 102 is connected to refresh unit 104 containing temperature processor 120 coupled to refresh timing 122 and row/column decoders sense amplifiers 124. *Id.* at 4:12–30. According to the '057 patent, "the DRAM array 112 may be implemented on a semiconductor chip and the temperature sensor 110 may be thermally coupled to the same semiconductor chip or to an intermediate member that is in thermal communication with the semiconductor chip." *Id.* at 4:22–26.

More specifically, in system 100 illustrated in Figure 3, upon receiving signal 116 from temperature sensor 110 indicating a temperature sensed from DRAM array 112, refresh unit 104 produces refresh signal 130 to refresh DRAM array 112 at a rate that varies in response to received temperature signal 116. *Id.* at 4:30–32. Preferably, DRAM array 112 is refreshed at a rate that decreases as the temperature of DRAM array 112 decreases. Conversely, DRAM array 112 is refreshed at a rate that increases

as the temperature of DRAM array 112 increases. *Id.* at 4:33–37. Further, according to the '057 patent, "the temperature sensor 110 and the DRAM array 112 are preferably disposed in a semiconductor package where the package includes at least one connection pin 117 operable to provide the signal on line 116 to external circuitry, such as the refresh unit 104." *Id.* at 4:49–53. "[T]he temperature sensor 110 preferably includes at least one diode 140 having a forward voltage drop that varies as a function of the temperature of the DRAM array 112." *Id.* at 5:17–20.

D. Illustrative Claim

Of the instituted claims, claims 1, 13, and 16 are independent. Claims 2–12 depend from independent claim 1. Claims 14 and 15 depend from independent claim 13. Claim 17 depends from independent claim 16. Independent claim is illustrative of the challenged claims, and is reproduced below:

> 1. An apparatus, comprising:
>
> a semiconductor package including at least one connection pin;
>
> at least one dynamic random access memory (DRAM) array disposed within the package; and
>
> at least one temperature sensor in thermal communication with the DRAM array, operable to produce a signal indicative of a temperature of the DRAM array, and coupled to the at least one connection pin such that the signal may be provided to external circuitry,
>
> wherein the DRAM array is refreshed at a rate that decreases as the temperature of the DRAM array decreases and that increases as the temperature of the DRAM array increases.

Ex. 1001, 5:60–6:7.

II. ANALYSIS

A. Claim Construction

The Board interprets claims of an unexpired patent using the broadest reasonable construction in light of the specification of the patent in which they appear. *See* 37 C.F.R. § 42.100(b); *see Cuozzo Speed Techs., LLC v. Lee*, 136 S. Ct. 2131, 2142–46 (2016). Under the broadest reasonable construction standard, claim terms are given their ordinary and customary meaning, as would be understood by one of ordinary skill in the art in the context of the entire disclosure. *In re Translogic Tech., Inc.*, 504 F.3d 1249, 1257 (Fed. Cir. 2007).

In our Decision on Institution, we found no material dispute between the parties as to claim construction in the present proceeding. Inst. Dec. 7.

Patent Owner contends that because Petitioner has not provided in the Petition how each of the challenged claims is to be construed, but instead advises the Board that the claims are to be construed according to their plain and ordinary meaning, Petitioner has failed to demonstrate a scope of the claimed invention that permits the Board to apply the asserted references to the claims. PO Resp. 13–14. Further, Patent Owner contends Petitioner previously argued in the companion district court litigation that the claim terms "refresh unit" and "refresh timing unit" in claims 6–11 are means plus function recitations with no corresponding structures in the Specification; that the cited claim terms are indefinite and cannot be construed. *Id.* at 16–17. According to Patent Owner, Petitioner cannot now request the Board to construe those claim terms as anything other than means plus function recitations. *Id.* at 17–18. Patent Owner, therefore, submits that Petitioner has failed to meet its burden to demonstrate, with reasonable certainty, the

scope of the claims to which the Board is to apply the alleged prior art. *Id.* at 18.

These arguments are not persuasive. Petitioner was not required to make explicit claim constructions for each term of each claim. "It may be sufficient for a party to provide a simple statement that the claim terms are to be given their broadest reasonable interpretation, as understood by one of ordinary skill in the art and consistent with the disclosure." Office Patent Trial Practice Guide, 77 Fed. Reg. 48,756, 48,764 (Aug. 14, 2012). For this reason, we disagree with Patent Owner's contention that Petitioner's statement that the claim terms be given their plain and ordinary meaning is insufficient. We also are not persuaded by Patent Owner's argument that Petitioner's position regarding its proposed claim constructions in the District Court for dependent claims 6–11 and prior allegation of indefiniteness of the cited claim terms in the district court proceeding "is a failure to meet its burden of proof." PO Resp. 18. We disagree that Petitioner's alleged inconsistent claim construction positions are fatal to Petitioner. Moreover, we decline Patent Owner's invitation to consider on the merits Petitioner's arguments made in the related District Court proceeding. PO Resp. 18. Here, neither party proffers an explicit construction of, or otherwise disputes the meaning of, any of the claim terms. We determine that it is not necessary to provide any express interpretation of the claim terms. Only terms that are in controversy need to be construed, and then only to the extent necessary to resolve the controversy. *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

B. Level of Ordinary skill in the Art

Both Petitioner's Declarant, Dr. Vivek Subramanian, and Patent Owner's Declarant, Dr. Joseph Bernstein, contend that a person having ordinary skill in the art at the time of the invention would have had (1) a Master's degree in Electrical Engineering, and (2) two to five years of experience working in the field of semiconductor design. Ex. 1005 ¶ 17, Ex. 2008 ¶ 25.

This definition is consistent with the level of ordinary skill reflected in the prior art references of record. *See Okajima v. Bourdeau*, 261 F.3d 1350, 1355 (Fed. Cir. 2001) (the prior art itself may reflect an appropriate level of skill in the art). ; *In re GPAC Inc.*, 57 F.3d 1573, 1579 (Fed. Cir. 1995); *In re Oelrich*, 579 F.2d 86, 91 (CCPA 1978). For purposes of this decision, we adopt the undisputed definition of the person of ordinary skill in the art, as set forth above.

C. The Parties' Post-Institution Arguments

In our Decision on Institution, we concluded that the arguments and evidence advanced by Petitioner demonstrated a reasonable likelihood that claims 1, 3, 5–9, 12, 13, and 16 of the '057 patent are unpatentable under 35 U.S.C. § 103(a) over the combination of Atkinson and Broadwater. Inst. Dec. 17. Further, we concluded that the arguments and evidence advanced by Petitioner demonstrated a reasonable likelihood that claims 2, 4, 10, 11, 14, 15, and 17 of the '057 patent under 35 U.S.C. § 103(a) are unpatentable over the combination of Atkinson, Broadwater, and Miller. *Id.* at 20. We must now determine whether Petitioner has established by a preponderance of the evidence that the specified claims are unpatentable over the cited prior art. 35 U.S.C. § 316(e).

With a complete record before us, we note that we have reviewed arguments and evidence advanced by Petitioner to support its unpatentability contentions where Patent Owner chose not to address certain limitations in its Patent Owner Response. In this regard, the record now contains persuasive, unrebutted arguments and evidence presented by Petitioner regarding the manner in which the asserted prior art teaches corresponding limitations of the claims against which that prior art is asserted. Based on the preponderance of the evidence before us, we conclude that the prior art identified by Petitioner teaches or suggests all uncontested limitations of the reviewed claims. The limitations of claim 1 and the limitations in the other challenged claims that Patent Owner contests in the Patent Owner Response are addressed below.

D. Obviousness over the Combination of Atkinson and Broadwater

Petitioner contends that claims 1, 3, 5–9, 12, 13, and 16 of the '057 patent are unpatentable under 35 U.S.C. § 103(a) over the combination of Atkinson and Broadwater. Pet. 12–32.

1. Principles of Law

A claim is unpatentable under § 103(a) if the differences between the claimed subject matter and the prior art are such that the subject matter, as a whole, would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 406 (2007). The question of obviousness is resolved on the basis of underlying factual determinations, including (1) the scope and content of the prior art; (2) any differences between the claimed subject matter and the prior art; (3) the level of skill in the art; and (4) when in evidence, objective indicia of non-obviousness

(i.e., secondary considerations). *Graham v. John Deere Co.*, 383 U.S. 1, 17–18 (1966). We analyze this asserted ground based on obviousness with the principles identified above in mind.

2. Atkinson Overview

Atkinson describes a technique for reducing the consumption of electric power in the main computer memory. Ex. 1010, 1:16–20. In particular, Atkinson discloses a refresh logic device that generates a memory refresh signal having a rate, which varies proportionally with the sensed temperature of the computer memory. *Id.* at 5:61–66, 7:41–44.

Figure 8 of Atkinson is reproduced below.

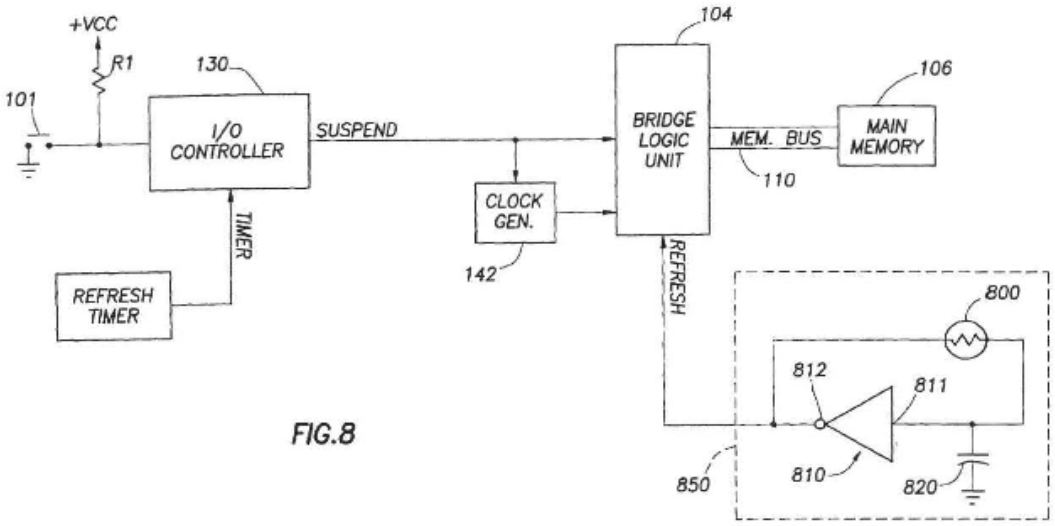

FIG.8

As illustrated in Figure 8 of Atkinson, refresh generator 850 includes thermistor 800, the temperature of which drops upon sensing a decreased temperature of main memory 106 to thereby produce a decrease of the rate of the refresh signal. *Id.* at 22:39–65. "Accordingly, the temperature of thermistor 800 represents the temperature of memory storage logic 930, and the refresh frequency decreases approximately in proportion to the decrease

in the temperature of memory storage logic 930." *Id.* at 24:11–17. Conversely, when the temperature of thermistor 800 increases upon sensing an increased temperature of main memory 106, refresh generator 850 increases the rate of the refresh signal. *Id.* at 7:41–44, 21:38–39. Atkinson also discloses an alternative embodiment in which refresh generator 950, including thermistor 800, is integrated in main memory 906. *Id.* at 23:37–40, 24:11–13, 24:22–23, Fig. 9.

Atkinson further discloses that that main memory 906 is an alternative embodiment of main memory 106 that preferably comprises DRAM circuitry (*id.* at 23:32–34), but may also be other types of DRAM, such as synchronous DRAM (SDRAM), extended data output DRAM (EDO RAM), and Rambus RAM. *Id.* at 3:38–46, 9:1–5. Main memory 106 is connected to bus 110 to exchange signals therewith. *Id.* at 12:4–7.

3. Broadwater Overview

Broadwater relates to a technique for sensing and reducing the effects of thermal stress on packaged semiconductor chips. Ex. 1006, 1:6–8, Abstract. Figure 1 of Broadwater is reproduced below:

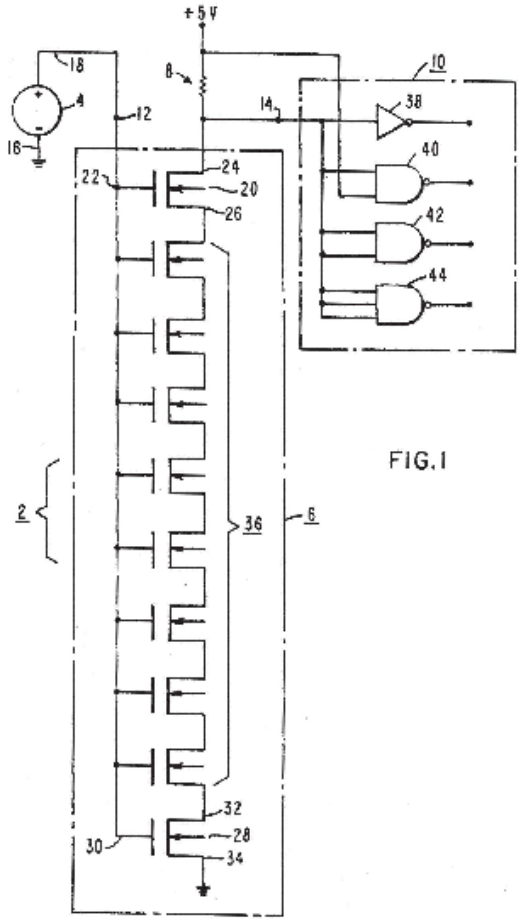

FIG. 1

As depicted in Figure 1 above, Broadwater describes a chip package having thermal stress sensing circuit 6 with input 12 and output 14. *Id.* at 3:35–37, 4:31–35. The voltage at output 14 varies as a function of input voltage and temperature. *Id.* at 4:39–41, Fig. 2. Output 14 can be routed to gate array 10, as shown, or can be provided to an external pin of the chip package. *Id.* at 4:31–53.

4. Petitioner's Positions

Petitioner asserts that the combination of Atkinson and Broadwater discloses the elements of claims 1, 3, 5–9, 12, 13, and 16. Pet. 12–32. We begin our analysis with claim 1. We have reviewed the Petition, Patent Owner Response, and Petitioner's Reply, as well as the relevant evidence

discussed in those papers and other record papers. We are persuaded that the record sufficiently establishes Petitioner's contentions for claims 1, 3, 5–9, 12, 13, and 16[5].

The preamble of claim 1 recites "an apparatus comprising." Ex. 1001, 5:61. Petitioner contends that Atkinson's description of an apparatus containing a main memory with a temperature sensor discloses the preamble of claim 1. Pet. 12.

Claim 1 next recites "a semiconductor package including at least one connection pin." Ex. 1001, 5:62–63. Petitioner contends that Atkinson's description of main memory 106 including any suitable type of memory such as DRAM or any of the special types of DRAM devices (e.g., SDRAM, EDO DRAM, Rambus DRAM) discloses the "semiconductor package" because "[o]ne of ordinary skill in the art would know that SDRAM and Rambus DRAM are packaged semiconductor chips." Pet. 13 (citing Ex. 1005 ¶ 41; Ex. 1007, 524; Ex. 1010, 4:31–35, 8:65–9:5). Further, Petitioner asserts that Atkinson's description of main memory 106's connection to bus 110 discloses the "connection pin" because one of ordinary skill would appreciate that "[a]s the main memory is composed of packaged memory chips that receive a variety of memory bus signals," its "connections to the memory bus 110 would necessarily require at least one connection pin or it would be obvious to have one." *Id.* at 13–14 (citing Ex. 1010, 12:4–7,

[5] We acknowledge Patent Owner's argument that "Dr. Subramanian's opinions on the ultimate question of obviousness are entitled to no weight" because he is not an attorney. PO Response 28–30. We arrive at the ultimate conclusion regarding obviousness independently and without adopting any purported "lay opinions" on the ultimate issue, *id.* at 28–29.

23:32–37, 12:8–12; Ex. 1005 ¶ 42). We are persuaded by Petitioner's showing and find that Atkinson's main memory 106 teaches a packaged semiconductor chip including at least one connection pin.

Claim 1 also recites "at least one dynamic random access memory (DRAM) array disposed within the package." Ex. 1001, 5:64–65. Petitioner asserts that Atkinson's description of a "computer system where the main memory 106 includes an array of memory devices such as DRAM" discloses the "package" having disposed therein the DRAM array. Pet. 14 (citing Ex. 1010, Figs. 1, 4A, 5, 7–9, 5:57–62, 8:37–9:15; Ex. 1005 ¶ 43). We are persuaded by Petitioner's showing and find that Atkinson's description of the main memory packaged in the semiconductor chip teaches a dynamic random access memory.

Claim 1 further recites "at least one temperature sensor in thermal communication with the DRAM array, operable to produce a signal indicative of a temperature of the DRAM array." Ex. 1001, 5:66–6:1. Petitioner asserts Atkinson's description of refresh generator 850, including thermistor 800 that directly senses the temperature of the DRAM, discloses "the temperature sensor . . . in thermal communication with the DRAM array." Pet. 14–16 (citing Ex. 1010, 22:52–62, 22:39–67, 23:32–37, 24:1–26, Fig. 8; Ex. 1005 ¶¶ 44, 45). Further, Petitioner asserts Atkinson describes an alternate embodiment wherein a "voltage controlled oscillator [(VCO)] combined with a temperature sensor could replace the refresh generator," such that "***the temperature sensor couples to main memory 106***, providing a voltage to the VCO ***that represents the main memory temperature***." *Id.* at 16 (citing Ex. 1010, 23:5–19). The refresh signal produced by the VCO varies with the temperature of the memory device as

sensed by the temperature sensor. *Id.* at 16–17 (citing Ex. 1010, 6:46–62, 7:46–48). We are persuaded by Petitioner's showing and find that Atkinson's description of the refresh generator, and alternatively the voltage controlled oscillator combined with the temperature sensor, teaches a sensor coupled to the DRAM array to indicate the temperature of the DRAM array.

Claim 1 also recites "coupled to the at least one connection pin such that the signal may be provided to external circuitry." Ex. 1001, 6:2–3. Petitioner asserts that Atkinson describes an on-chip embodiment wherein a temperature sensor coupled directly to main memory 106 provides a voltage to the VCO that represents the main memory temperature. Pet. 17 (citing Ex. 1010, 23:15–17, Fig. 8; Ex. 1005 ¶ 47). According to Petitioner, while the on-chip embodiment described by Atkinson does not disclose providing the temperature signal to an external circuit, such a modification would have been obvious to one of ordinary skill in the art, particularly in view of Broadwater's disclosure of an external pin of a chip package (e.g., DRAM memory chip) for outputting a signal indicative of the chip's temperature. *Id.* (citing Ex. 1005 ¶¶ 47–49); *id.* at 30 (citing Ex. 1006, 4:31–33, 4:49–53; Ex. 1005 ¶¶ 83–84).

Further, Petitioner asserts that the ordinarily skilled artisan would have been motivated to combine the cited disclosures of Atkinson and Broadwater because Broadwater's disclosure of adding an external pin to an existing chip package (e.g., Atkinson's DRAM) would help reduce the effects of thermal stress on the DRAM. *Id.* at 31 (citing Ex. 1006, 1:14–29; Ex. 1005 ¶ 85). Additionally, Petitioner concludes that the ordinarily skilled artisan would have recognized that the proposed combination would help maximize power saving during the self-refresh timing sequence. *Id.* (citing

Ex 1005 ¶ 86). We are persuaded that a person having ordinary skill in the art would have found it obvious to combine the teachings of Atkinson and Broadwater because we agree that transmitting the sensed temperature of the DRAM to an external circuit via an external pin would have been recognized by a person having ordinary skill in the art as resulting in a more efficient system that maximizes power saving by reducing thermal stress on the packaged semiconductor chip.

Claim 1 also recites "wherein the DRAM array is refreshed at a rate that decreases as the temperature of the DRAM array decreases and that increases as the temperature of the DRAM array increases." Ex. 1001, 6:4–7. Petitioner asserts Atkinson describes a refresh logic that reduces the rate of the refresh signal in response to receiving a signal from the temperature sensor indicating a drop in the main memory temperature. Pet. 19 (citing Ex. 1010, 13:13–15, 22:2–7). Conversely, the refresh logic increases the rate of the refresh signal in response to receiving a signal indicating an increase in the temperature of the main memory. *Id.* (citing Ex. 1010, 7:41–44; Ex. 1005 ¶¶ 50–51). According to Petitioner, the refresh frequency increases or decreases in proportion to the increase or decrease in the temperature of the DRAM as a way to achieve the greatest power savings. *Id.* (citing Ex. 1010, 20:53–56, 24:3–17, Fig. 6; Ex. 1005 ¶ 51). We are persuaded by Petitioner's showing and find that Atkinson's description of the refresh logic teaches a mechanism for providing to the DRAM an increased or decreased refresh rate in proportion with the sensed temperature of the DRAM.

Independent claims 13 and 16 are similar to claim 1. Petitioner has made a showing with respect to claims 13 and 16 similar to its showing with

respect to claim 1. *See, e.g.*, Pet. 26–28. To the extent that claims 13 and 16 are different from claim 1, Petitioner has accounted for such differences. We also have reviewed Petitioner's showing with respect to dependent claims 3, 5–9, and 12. *Id.* at 21, 23–26. Notwithstanding Patent Owner's arguments, which we have considered and which we address below, we are persuaded by Petitioner's showing, which we adopt as our own findings and conclusions, as set forth above, that claims 1, 3, 5–9, 12, 13, and 16 are unpatentable as obvious over the combination of Atkinson and Broadwater.

5. Patent Owner's Assertions Concerning the References

Patent Owner argues that the challenged claims would not have been obvious over the combination of Atkinson and Broadwater for the following reasons: (a) "Petitioner does not demonstrate a proper motivation to modify Atkinson to add Broadwater's 'connection pin' to provide a temperature indicative signal to 'external circuitry,'" as recited in challenged claims 1–17 (PO Resp. 32–53 (emphasis omitted)); (b) "Petitioner has failed to show it was obvious to modify Atkinson to add the 'diode' limitations," as recited in dependent claims 2, 4, 10, 11, 14, and 15 (*id.* at 19–27, 53–57 (emphasis omitted)); and (c) "Petitioner has failed to point out where the 'refresh unit' . . . and 'refresh timing unit' . . . limitations are found," as recited in dependent claims 6–11, and 7–11 respectively (*id.* at 57–60). We address each argument in turn.[6]

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[6] Patent Owner lists several portions of Petitioner's Reply and evidence as being allegedly beyond the scope of what can be considered appropriate for a reply. *See* Paper 23. We have considered Patent Owner's listing, but disagree that the cited portions of Petitioner's Reply and reply evidence are

a. The Allegation that Petitioner Does Not Demonstrate a Proper Reason to Modify Atkinson to Add Broadwater's "Connection Pin" to Provide a Temperature Indicative Signal to "External Circuitry" (claims 1–17)

Independent claim 1 recites, in relevant part, "at least one connection pin such that the signal may be provided to external circuitry." Independent claim 13 recites, in relevant part, "at least one connection pin operable to provide the signal to external circuitry." Independent claim 16 recites, in relevant part, "outputting a signal indicative of the temperature of the DRAM array to external circuitry." Patent Owner presents four sub-arguments: (i) "The teachings of Atkinson and Broadwater discourage the combination" (PO Resp. 37–42 (emphasis omitted)); (ii) "Even if Atkinson and Broadwater were not contrary to the Patent's teaching, there is no reason to combine them to make the specific invention claimed" (*id.* at 42–47 (emphasis omitted)); (iii) "The proposed Atkinson-Broadwater combination would require extensive modifications of Atkinson to practice the claims" (*id.* at 48–50 (emphasis omitted)); and (iv) "Petitioner and its declarant wave aside the references' disclosures and rely on generalities and offhand

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beyond the scope of what is appropriate for a reply. Replies are a vehicle for responding to arguments raised in a corresponding patent owner response. Petitioner's arguments and evidence that Patent Owner objects to (*id.* at 1) are not beyond the proper scope of a reply because we find that they fairly respond to Patent Owner's arguments raised in Patent Owner's Response. *See Idemitsu Kosan Co., Ltd. v. SFC Co. Ltd.*, 870 F.3d 1376, 1381 (Fed. Cir. 2017) ("This back-and-forth shows that what Idemitsu characterizes as an argument raised 'too late' is simply the by-product of one party necessarily getting the last word. If anything, Idemitsu is the party that first raised this issue, by arguing—at least implicitly—that Arakane teaches away from non-energy-gap combinations. SFC simply countered, as it was entitled to do.").

comments in each reference" (*id.* at 50–53 (emphasis omitted)). We address each in turn.

i. Whether the teachings of Atkinson and Broadwater Discourage the Combination.

Patent Owner argues that "[t]here is no motivation to couple Atkinson's onboard sensor to a connection pin such that the temperature indicative signal may be provided to external circuitry, because in Atkinson all external circuitry, particularly any that might affect the DRAM refresh rate, is expressly turned off." PO Resp. 37 (citing Ex. 1010, 4:54–59, 6:6–10, 11:4–16). Specifically, Patent Owner argues that every embodiment disclosed in Atkinson is focused on performing the refresh operation during system sleep with all external logic/circuitry outside of the DRAM module off. *Id.* According to Patent Owner, modifying Atkinson's onboard module in its sleep state (during which the rate of temperature decreases to control the DRAM refresh rate) to operate with an external circuitry in active state, would go against the thrust of Atkinson. *Id.* (citing Ex. 2008 ¶ 60). Patent Owner stresses that Atkinson's "on-chip" embodiment with the temperature sensor in thermal communication with the array was designed to be self-contained to include the temperature sensing refresh generator within main memory 906. *Id.* at 38 (citing Ex. 1010, 24:22– 23, 24:23–27; Ex. 2008 ¶ 61). Further, Patent Owner argues that the "on-chip" embodiment does not include a connection pin to provide a signal indicative of the DRAM temperature to an external circuit because, in response to the temperature, it generates internally a refresh pulse, which does not provide meaningful data based on the temperature sensor by a pin to an external circuitry. *Id.* (citing Ex. 1010, Fig. 8, 22:38–23:1). Furthermore, Patent Owner argues that adding components to Atkinson's "on-chip" embodiment with its on-board

components would have increased the price, size, and complexity of the unit. *Id.* at 39 (citing Bernstein ¶ 63). Additionally, Patent Owner argues that Broadwater is not related to memory, DRAM or refresh, and offers no tradeoffs or incentives for additional on-board circuitry or pins for which the solution is to reduce or cutoff circuit activity (as opposed to increasing circuit activity). *Id.* at 39–40 (citing Ex. 1006, 5:18–32). According to Patent Owner, Broadwater is concerned with combatting thermal stress from operating temperatures during operation. *Id.* at 40 (citing Ex. 1006, 1:30–51, 4:66–5:1). In Patent Owner's words, "while Atkinson is on, Broadwater is off, and vice versa." *Id.* (citing Ex. 2008 ¶¶ 63–66). Patent Owner argues that Atkinson and Broadwater are directed to very different applications. In particular, Atkinson is directed to making power use more efficient in laptops during system sleep, whereas Broadwater is directed to protecting mission critical circuitry in high speed aircraft. *Id.* (citing Ex. 1010, 3:6–28; Ex. 1006, 1:25–31).

Moreover, Patent Owner argues that although both Atkinson and Broadwater are focused on power efficiency, they do so by reducing circuit activity, whereas the '057 patent reduces waste of energy by increasing circuit activity. *Id.* at 40–41. That is, Atkinson prevents waste of energy by dropping circuit activity from a default level when the temperature drops, and Broadwater prevents waste of energy by dropping circuit activity from a default level when the temperature increases. *Id.* at 41 (citing Ex. 1010, 13:11–18; Ex. 1005, 5:18–27). In contrast, Patent Owner stresses that the '057 patent prevents waste of energy and failure by increasing circuit activity from a default level when the temperature increases. *Id.* (citing Ex. 1001, 3:55–66; Ex. 2008 ¶¶ 69–70). Therefore, Patent Owner submits that

both Atkinson and Broadwater disclose cutting the temperature of the circuits, whereas the '057 patent teaches increasing the circuitry temperature most when it is at its hottest. *Id.* (citing Ex. 1006, 5:18–27; Ex. 1010, 13:11–18;, Ex. 1001, 2:34–36, 3:55–58; Ex. 2008 ¶ 71).

A further difference argued by Patent Owner is that Atkinson is active when the external circuit is not operational, whereas the '057 is active when the external circuit is operational. *Id.* (citing Ex. 1010, 3:6–28; Ex. 1001, 2:1–2, 2:64–67; Ex. 2008 ¶ 72). Likewise, Patent Owner argues that Broadwater teaches shutting down part of the circuit, whereas the '057 "patent teaches keeping its DRAM active and working, since shutting down any portion would amount to a total data loss of that portion." *Id.* (citing Ex. 1006, 1:25–45; Ex. 1001, 1:51–59; Ex. 2008 ¶ 73).

Petitioner counters that Atkinson and Broadwater are directed to the same field of endeavor. Reply 2 (citing Ex. 1018, 38:3–6). According to Petitioner, chiefly among the ample reasons why a person of ordinary skill in the art would add Broadwater's functionality of reducing thermal stress in chips to Atkinson's circuitry is to prevent the DRAM in Atkinson from "blowing up" thereby furthering Atkinson's purpose of ensuring reliable operation of the chip. *Id.* at 2–3. Petitioner contends that because nothing in the claims requires the external pin to be used as part of the refresh process, there is no basis in the claims to support Patent Owner's argument that a temperature pin cannot be added to Atkinson's system, which performs the refresh process in a sleep mode. *Id.* at 3–4, 8. In particular, Petitioner argues because Atkinson's chip is still functioning even when it is in sleep mode, it is still subject to overheating. *Id.* at 4. Therefore, Petitioner submits that the ordinarily-skilled artisan would have good reason to add the

overheat protection of Broadwater to Atkinson's circuitry during periods of sleep mode and in the wake state because the external pin is not limited to a particular state. *Id.*

We agree with Petitioner. First, we agree with Petitioner that Atkinson and Broadwater are within the same field of endeavor because both references are generally within the field of integrated circuits. Reply 2. In particular, the references relate to optimizing the performance of integrated circuits by preventing the overheating thereof thereby enhancing reliability, temperature, and power consumption of integrated circuits. Further, Patent Owner's arguments regarding Atkinson are not commensurate in scope with the claim language. Patent Owner has not provided any basis in the claims to support the argument that Atkinson's system cannot be modified as proposed to add an external connection pin to complement the refresh process. The claim recitation "one connection pin such that the signal may be provided to external circuitry" implies that the external pin may be used as a vehicle for indicating the temperature of the DRAM to the external circuitry. However, as persuasively argued by Petitioner, the cited claim limitation does not restrict the use of the external pin/circuit to a particular state. Nor does it tie the external pin to the refresh process triggered in response to being informed of the DRAM temperature. As correctly noted by Petitioner, so long as Atkinson's DRAM is subject to disrupted operation due to possible overheating (in the sleeping mode or wake state) and includes a temperature sensor that outputs the sensed temperature of the DRAM, its proposed combination with Broadwater would be proper because Broadwater's thermal stress reduction technique would help cool down the chip notwithstanding that the systems of Atkinson and Broadwater operate at

different states. *Id.* at 4–5, 10. Accordingly, we agree with Petitioner that the teachings of Atkinson and Broadwater do not discourage the proposed combination.

ii. Whether Even If Atkinson and Broadwater Were Not Contrary to The Patent's Teaching, There Is No Reason to Combine Them to Make the Specific Invention Claimed.

Patent Owner argues that there is no reason to modify Atkinson to provide signals indicative of the onboard array temperature from the DRAM array to an external circuitry using Broadwater's external pin. PO Resp. 42 (citing Ex. 2008 ¶ 75). According to Patent Owner, adding an external pin to an existing DRAM is a very expensive and complex endeavor that counters the intended operation of Atkinson's self-refresh chip. *Id.* Patent Owner contends that because Atkinson's system performs an internal refresh operation in the sleep mode, the additional expense and complexity associated with adding an external pin would not be justified. *Id.* at 43–44. Moreover, Patent Owner contends that adding a forward biased diode as the temperature sensor would further increase the energy drain "sleep" mode. *Id.* at 44 (citing Ex. 2008 ¶¶ 78–79). Additionally, Patent Owner argues that neither Atkinson nor Broadwater discloses any teachings pertaining to external control of DRAM timing to facilitate efficient, deterministic control of the DRAM in sync with the rest of the activity of the system. *Id.* at 45–46 (citing Ex. 2008 ¶ 82).

These arguments are not persuasive. As correctly noted by Petitioner, because the claims do not recite any limitation regarding external control of DRAM timing, Patent Owner's arguments are misplaced and are not commensurate with the scope of the claims. Reply 8. Further, we agree with Petitioner that adding a pin to Atkinson's chip for the purpose of

communicating the sensed temperature of the DRAM to the external circuit, as taught by Broadwater, was well within the purview of the ordinarily-skilled artisan. *Id.* at 6–7, 9–10. As acknowledged by Patent Owner, Broadwater's disclosed technique pertains to a refresh circuit producing a refresh signal to reduce thermal stress in an integrated circuit (e.g., Atkinson's DRAM) in response to receiving from an external pin a signal indicating thermal distress in the chip. PO Resp. 36 (citing Ex. 1006, 2:31–38). Thus, we agree with Petitioner that because Broadwater's teachings pertain to relieving any type of chips from thermal distress, the ordinarily-skilled artisan would have been apprised that such a communication of the sensed temperature of the DRAM to the external circuitry via the external pin is a suitable addition to complement Atkinson's refreshing circuit in relieving the DRAM from possible overheating. Pet. 31 (citing Ex. 1005 ¶¶ 85, 86); Reply 7–8. Accordingly, we agree with Petitioner that there are sufficient reasons to combine the teachings of Atkinson and Broadwater to yield the specific invention claimed. Reply 3–4.

iii. Whether the Proposed Atkinson-Broadwater Combination Would Require Extensive Modifications of Atkinson to Practice the Claims.

Patent Owner asserts that "a combination of Atkinson and Broadwater to practice the claims would require extensive modifications." PO Resp. 48. Specifically, Patent Owner argues that the proposed modification of Atkinson to add a connection pin would be extensive. *Id.* In particular, Patent Owner argues that such modification would require (1) selecting Atkinson's non-preferred embodiment with an on-chip temperature sensor in direct communication with the DRAM; (2) removing the temperature-sensing refresh generator from main memory so as to justify providing the

signal to external circuitry; (3) adding a connection pin to the on-chip DRAM module; (4) generating a signal indicative of temperature that may be provided over the pin; (5) having the external circuitry in active mode while its energy saving system is working (not in sleep mode); (6) adding logic permitting DRAM to be refreshed at higher than default operation rate in high temperature situations; and (7) replacing temperature sensor with forward-biased diode. *Id.* at 48–50 (citing Ex. 2008 ¶¶ 85–91).

These arguments are not persuasive. We agree with Petitioner that none of these arguments has any basis in the claims. Reply 9. Further, we do not find any support on this record that Petitioner's proposed combination of Atkinson and Broadwater would require the cited modifications above, as alleged by Patent Owner in reliance upon Dr. Bernstein's Declaration. The alleged modifications are incorrectly premised upon the substitution of Atkinson's onboard refresh unit with Broadwater's external refresh unit. Instead, the modification proposed by Petitioner contemplates adding a pin to Atkinson's on-board circuit to communicate the sensed temperature of the DRAM to the external circuit. Pet. 17 (citing Ex. 1005 ¶¶ 47–49); *id.* at 30 (citing Ex. 1006, 4:31–33, 4:49–53; Ex. 1005 ¶¶ 83–84). Consequently, the resulting Atkinson-Broadwater system would offer the dual benefit of maximizing power saving during self-refresh timing sequence, as well as reducing thermal stress on the DRAM. *Id.* at 31 (citing Ex. 1006, 1:14–29; Ex. 1005 ¶¶ 85–86). Therefore, we agree with Petitioner that none of these arguments changes the conclusion that the proposed modification of Atkinson with Broadwater would reinforce Atkinson's onboard refresh unit thereby allowing Atkinson's system to combat both thermal distress and preserve energy consumption. Reply 2–3 (citing Ex. 1018, 38:3–6, 40:5–15,

20–25). Furthermore, we agree with Petitioner that because the laptop disclosed in Atkinson is vulnerable to overheating even in sleep mode, it could benefit from Broadwater's external refresh unit, which is designed to relieve such circuit from thermal distress irrespective that the latter external unit operates in the active mode. *Id.* at 10. Moreover, we agree with Petitioner because Atkinson discloses a system configured to increase or decrease the DRAM refresh rate proportionally with the sensed temperature of the DRAM, a person of ordinary skill in the art (POSITA) would have been motivated to supplement Atkinson's circuitry with Broadwater's external refreshing circuit as a way to keep the DRAM operating at all times. *Id.* at 10–11. On this record, we are not persuaded that the proposed Atkinson-Broadwater combination would require extensive modifications of Atkinson to practice the claims.

iv. Whether Petitioner and Its Declarant Wave Aside the References' Disclosures and Rely on Generalities and Offhand Comments in Each Reference

Patent Owner alleges that both Petitioner and its declarant rely on virtual irrelevancies, instead of main teachings from the references, in an attempt to show a motivation to combine the references. PO Resp. 51. In particular, Patent Owner offers the following examples of alleged generic Petitioner's statements: "it is desirable for the computer or external circuitry to be aware of the temperature for thermal management reasons," "to 'monitor and track the memory temperature for diagnostic purposes,'" "to enable throttling of power to reduce heat." *Id.* According to Patent Owner, such statements are conclusory and "would apply to anything that uses temperature as an input." *Id.* Further, Patent Owner argues that "Petitioner's declarant, at deposition, ignored or waved away most of the

disclosures of both references in order to dwell on minute offhand comments in both references that he argued lend purported support to the combination." *Id.* at 52. In particular, Patent Owner argues that Petitioner's declarant, Dr. Subramanian, "dwelled [at his deposition] on Broadwater's asides" such as concepts that might be useful at low temperatures (*id.* (citing Ex. 2009, 147:24–148:21, 160:16–165:2)); whereas "Broadwater is directed to alleviating thermal stress from overheating circuitry by selectively shutting off parts of the overheated circuitry to reduce its temperature." *Id.* (citing Ex. 1006 1:14–45, 3:48–64, 5:35–45). Likewise, Patent Owner argues that "Atkinson is wholly directed to DRAM low-temperature self-refresh in non-operation;" whereas declarant's deposition "dwelled" on the comment that in Atkinson "'the refresh rate may be varied according to temperature during normal computer operation.'" *Id.* at 52–53 (citing Ex. 1010, 6:5–8; Ex. 2009, 175:12–176:10, 182:14–24). Patent Owner, therefore, submits that none of these off-hand comments corresponds to any explicit embodiments or substantial teachings in the references about how the completed applications might be accomplished. *Id.* at 53 (citing Ex. 2008 ¶¶ 95–98).

These arguments are not persuasive. We agree with Petitioner that the asserted motivation statements are not generalities, but pertain to reasons why a POSITA would have combined the teachings of Atkinson with Broadwater's. Reply 12. In particular, we agree with Petitioner that, as taught in Broadwater, thermal stress reduction during the operation of integrated chips has been recognized in the semiconductor art as a significant problem to be addressed. *Id.* (citing Pet. 30; Ex. 1006, 1:14–22). Likewise, we agree with Petitioner that even Patent Owner's expert

acknowledges the benefit of preventing ICs from "blowing up." *Id.* at 13 (citing Ex. 1018, 40:12–15, 141:7–12).

On the record before us, we are persuaded that there is adequate motivation to modify Atkinson's sensor to add Broadwater's connection pin so as to provide a signal indicative of the DRAM sensed temperature to an external circuitry for the purpose of reducing thermal stress in Atkinson's integrated circuit.

For the foregoing reasons, we are persuaded that Petitioner has established, by a preponderance of the evidence, that claims 1, 3, 5–9, 12, 13, and 16 of the '057 patent are unpatentable under 35 U.S.C. § 103(a) over the combination of Atkinson and Broadwater.

b. The Allegation That "Petitioner Has Failed to Show it Was Obvious to Modify Atkinson to Add the 'Diode' Limitations" (claims 2, 4, 10, 11, 14, 15, and 17)

Dependent claims 2, 4, 10, 11, 14, 15, and 17 recite, in relevant part, "wherein the at least one temperature sensor includes at least one diode having a forward voltage drop that varies as a function of the temperature of the DRAM array, and the signal corresponds to the forward voltage drop of the at least one diode." Ex. 1001, 6:8–12.

1. Petitioner's Positions

Petitioner contends claims 2, 4, 10, 11, 14, 15, and 17 are unpatentable under 35 U.S.C. § 103(a) as being unpatentable over the combination of Atkinson, Broadwater, and Miller.[7] Pet. 20–21, 22, 25, 27,

[7] Although Miller is omitted from the Petition's summary of asserted grounds, it was nevertheless relied upon in Petitioner's analysis of claims 2, 4, 10, 11, 14, 15, and 17. *See, e.g.*, Pet. 20. We, therefore, in the Decision

28, 29–30. Relying on the declaration of Dr. Subramanian, Petitioner explains how the proposed combination of references discloses all of the claim limitations. *Id.* (citing Ex. 1005). In particular, Petitioner asserts that, although the '057 patent includes a diode as a known temperature sensor, it also discloses other known temperature sensors (e.g., thermocouples, thermistors, or any other device that provides an output signal varying as a function of temperature). Pet. 20 (citing Ex. 1001, 2:42–45). Petitioner further asserts that Atkinson similarly discloses the use of such known temperature sensors (e.g., thermocouple or temperature sensing integrated circuit). *Id.* (citing Ex. 1010, 22:21–24; Ex. 1005 ¶¶ 52, 53). Petitioner then contends that, at the time of the invention, measuring a forward voltage drop across a semiconductor diode to thereby read the temperature, as described in Miller, was a well-known use of such a type of temperature sensor. Pet. 20 (citing Ex. 1015, Abstract). Petitioner concludes it would have been obvious to one of ordinary skill in the art to select a diode as a well-known type of temperature sensor for reading the temperature of Atkinson's DRAM. *Id.* at 21 (citing Ex. 1010, 24:63–65; 1005 ¶ 53). We are persuaded by Petitioner's showing and find that Miller's description of a diode as a temperature sensor would complement the Atkinson-Broadwater combination to teach using the diode to sense the temperature of the DRAM, which is communicated to an external circuitry via an external pin.

Likewise, claim 4 depends directly from claim 1, and recites

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on Institution treated Petitioner's analysis of claims 2, 4, 10, 11, 14, 15, and 17 based upon Atkinson, Broadwater, and Miller as a separate ground of unpatentability. Inst. Dec. 5.

> wherein the at least one temperature sensor includes a diode having a forward voltage drop that varies as a function of the temperature of the DRAM array; the at least one connection pin includes a first pin coupled to an anode of the diode and a second pin coupled to a cathode of the diode; and the signal corresponds to a potential voltage between the first and second pins.

Ex. 1001, 6:17–23. Petitioner explains, with supporting evidence, that at the time of the invention, "given that the claim merely recites 'first pin' and 'second pin,' the diode temperature sensor would necessarily be connected to a first pin and a second pin if it were operational." Pet. 22 (citing Ex. 1005 ¶ 56). Petitioner further explains that "in such a diode configuration, the signal between the first pin and the second pin would necessarily be the forward voltage drop of the diode, which claim 4 defines as the signal." *Id.* Petitioner concludes that it would have been obvious to one of ordinary skill in the art at the time of the invention to "modify Atkinson to use a diode configuration as recited in claim 4 (which is essentially the same as the obvious variant in claim 2)." *Id.* We are persuaded by Petitioner's showing and find that Miller's diode coupled to the pins in Atkinson's DRAM teaches a forward biased diode connected to the connection pins.

We also have reviewed the Petition with respect to dependent claims 10, 11, 14, 15, and 17, and determine that Petitioner has accounted sufficiently for the recited limitations. Pet. 25, 27, 28.

2. Patent Owner's Assertions Regarding the References

Patent Owner makes two principal arguments: (i) Miller was not part of any of the combinations expressly raised by the Petition (PO Resp. 19–28), and that (ii) Petitioner fails to show it was obvious to modify Atkinson

to add the diode limitations. *Id.* at 53–57. We address each argument in turn.

i. The Allegation that Miller was not Part of Any Combination Expressly Raised in the Petition

Patent Owner argues that Petitioner did not expressly raise Miller as part of any of the combinations argued in the Petition. PO Resp. 54. In particular, Patent Owner argues that the Petition's "Summary of Grounds of Rejection" lists Atkinson and Broadwater as a possible combination, but never mentions Miller. *Id.* at 20. According to Patent Owner, while the Petition recognizes that the Atkinson-Broadwater combination is silent about the forward biased diode, it asserts that the ordinarily-skilled artisan would have known that forward biased diodes were well-known in the art for sensing temperature, and then lists Miller as an example of such common use of forward biased diode. *Id.* According to Patent Owner, such a reference to Miller in the Petition is not tantamount to including Miller as part of the Atkinson-Broadwater combination. *Id.* at 21. Patent Owner argues that the Board, *sua sponte*, redrafted the ground of unpatentability proposed by Petitioner to yield the Atkinson, Broadwater, and Miller combination as a separate and new ground in the Institution Decision thereby converting Miller from background art to a reference in the combination. *Id.* at 19, 21–22. Consequently, Patent Owner submits that by instituting on the new ground combination, the Board has caused the following:

(1) Deprived Patent Owner of its due process right to file a preliminary response as to the new ground (PO Resp. 23–24);

(2) Violated the Board's regulations whereby the Petition must identify the challenge along with the specific ground (*id.* at 24–25);

(3) Contradicted without reason Petitioner's choice of making Miller background art, as opposed to making Miller part of the combination (*id.* at 25);

(4) Prejudiced Patent Owner by forcing it to consider and address the issue in its Patent Owner's Response (*id.* at 26); and

(5) Contravened the Administrative Procedure Act's requirement to maintain an impartial stance by weighing on Petitioner's side of the controversy (*id.* at 26–28).

In response, Petitioner argues that Miller is introduced in Ground 1 of the Petition to teach using a diode detecting temperature in an integrated circuit. Reply 15 (citing Pet. 19–20). According to Petitioner, because Ground 2 builds off Ground 1, the Board properly interpreted Petitioner's intent to make Ground 2 additive to Ground 1, and therefore to include Miller, and that the heading or title within the Petition does not alter the underlying content of the Petition. *Id.* at 14–15.

We agree with Petitioner. As noted in the Institution Decision, Petitioner's discussion of Miller within the content of the Petition as a way to bolster the Atkinson-Broadwater combination is tantamount to the Atkinson-Broadwater-Miller combination. Inst. Dec. 5; Pet. 20–21. Patent Owner was apprised of the Petitioner's reliance on Miller in the Petition, and Patent Owner availed itself of the opportunity to provide arguments addressing Miller in the Patent Owner Response (*see* PO Resp. 53–57). Accordingly, we are not persuaded that the combination of Atkinson, Broadwater, and Miller was not raised in the Petition.

ii. The Allegation that There is No Motivation to Combine Miller with Atkinson

Patent Owner argues that because Miller does not discuss memory, DRAM, or DRAM refresh, substituting Miller's forward-voltage-drop diode for Atkinson's thermistor would not have been obvious to the ordinarily-skilled artisan. PO Resp. 54. According to Patent Owner, neither the Petitioner nor its declarant identifies a rationale supporting the proposed substitution of Atkinson's temperature sensors for Miller's diode. *Id.* at 55. Patent Owner further argues that merely indicating Miller's diode could be selected over the alternatives listed in Atkinson does not identify a rationale for the proposed substitution. *Id.* (citing Ex. 2008 ¶¶ 99–101). Furthermore, Patent Owner argues that because the claimed diode voltage sensor only works with the diode forward biased, the steady state current flowing through a voltage drop for sensing the temperature through the forward-biased diode would increase the steady state power during the sleep mode. *Id.* Accordingly, Patent Owner submits that a diode would increase the sleep mode current drain, and would thereby violate Atkinson's desired reduction in energy consumption. *Id.* Additionally, Patent Owner argues that even if Miller were used as merely background information as intended by Petitioner, the Petition still fails to show that it would have been obvious to replace a generally known diode in place of Atkinson's thermistor because the limitation in question is not "'unusually' insignificant" and the technology "'particularly straightforward.'" *Id.* at 56. Patent Owner, therefore, submits that because the diode limitations are important structural limitations in the claim, replacing Atkinson's thermistor with Miller's generally known diode would change the operation of the device and necessitates modification of Atkinson's refresh generator. *Id.* at 57.

Petitioner counters that because diodes have been used for sensing temperature in integrated circuits since the 1970s, POSITA would have known that the proposed substitution is reasonable as conceded by Patent Owner's expert. Reply 13–14 (citing Ex. 1010, 22:21–26; Ex. 2009, 209:12–17; Ex. 1015; Ex. 1018, 188:19–25), 18–19. In particular, Petitioner argues that Broadwater's express teaching of using a diode to detect temperature (Ex. 1006, 3:55–58), taken in combination with Patent Owner's admission that a thermocouple is much like a forward biased diode (Ex. 1018, 180:6–10) supports the proposed combination. *Id.* at 14. Further, Petitioner submits that "[o]ne of ordinary skill in the art would be motivated to send the signal indicative of memory temperature to an external connection pin, at least to enable its use in a cooling regime, such as the one set forth in Miller." Pet. 18. Additionally, Petitioner submits "[t]hose of ordinary skill at the time of the filing of the '057 [p]atent would know that one example of the finite alternate types of integrated circuits for detecting temperature was a diode having a forward voltage drop that varies as a function of temperature." *Id.* at 20.

We agree with Petitioner. As correctly argued by Petitioner, Patent Owner does not dispute that, at the time of the invention, using a diode for sensing the temperature of an integrated device was well-known in the art. Therefore, we agree with Petitioner that although Miller is not related to a memory type circuit, the forward-biased diode disclosed in Miller is directed to sensing integrated circuits as a whole including memory integrated circuits such as the DRAM disclosed in Atkinson. Reply 15–17. Further, as correctly noted by Petitioner, Atkinson, in fact, suggests using alternative temperature sensing devices not particularly listed for sensing the

temperature of the DRAM. Pet. 20 (citing 1010, 22:21–24). Furthermore, we do not agree with Patent Owner that Petitioner has not provided sufficient motivation for substituting Miller's forward biased diode with Atkinson's thermistor. As noted above, Petitioner expressly asserts that the ordinarily-skilled artisan would have made the proposed substitution to enable the use of Atkinson's DRAM in a "cooling regime," as well as "to enable throttling of power to reduce heat as well as to monitor and track the memory temperature for diagnostic purposes." Pet. 18. Moreover, as discussed above, irrespective of differing modes of Atkinson's DRAM, Broadwater's external circuit or Miller's forward biased diode, the overall combination of the cited references would predictably result in reducing thermal stress in the DRAM, upon being notified that the DRAM is overheating, thereby reducing the overall power consumption of the circuit. In other words, Petitioner's proposed combination of the cited teachings of Atkinson, Broadwater, and Miller is no more than a simple arrangement of old elements with each performing the same function it had been known to perform, yielding no more than one would expect from such an arrangement. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 416 (2007). The ordinarily-skilled artisan, being "a person of ordinary creativity, not an automaton," would be able to fit the teachings of the cited references together like pieces of a puzzle to predictably result in an external circuit that provides a proportional cooling signal to a DRAM circuit upon receiving a signal from a forward biased diode indicating a sensed temperature of the DRAM. *Id.* at 420–21. We are not persuaded that the Petitioner's proffered combination would have been "uniquely challenging or difficult for one of ordinary skill in the art"; we agree with the Petitioner that the proposed modification

would have been within the purview of the ordinarily skilled artisan. *Leapfrog Enters., Inc. v. Fisher-Price, Inc.*, 485 F.3d 1157, 1162 (Fed. Cir. 2007) (citing *KSR*, 550 U.S. at 418).

Petitioner has sufficiently shown that it would have been obvious to use the diode described in Miller to read and measure the temperature of Atkinson's DRAM. Pet. 20–21. On the record before us, we are persuaded that Petitioner has provided an articulated reasoning with some rational underpinning sufficient to support the legal conclusion of obviousness based on Atkinson, Broadwater, and Miller. *See KSR*, 550 U.S. at 418.

For the foregoing reasons, we are persuaded that Petitioner has established, by a preponderance of the evidence, that claims 2, 4, 10, 11, 14, 15, and 17 of the '057 patent are unpatentable under 35 U.S.C. § 103(a) over the combination of Atkinson, Broadwater, and Miller.

c. The Allegation that Petitioner Has Failed to Point Out Where the "Refresh Unit" (Claims 6–11) and the "Refresh Timing Unit" (Claims 7–11) Limitations Are Found.

Dependent claims 6–11 recite, in relevant part, "a refresh unit operable to refresh the DRAM array at a rate that varies in response to the signal." Ex. 1001, 6:28–30. Further, dependent claims 7–11 recite a "refresh timing unit is operable to decrease the rate at which the DRAM array is refreshed as the signal indicates that the temperature of the DRAM array decreases." *Id.* at 6:36–39.

1. Petitioner's Positions

Petitioner asserts Atkinson describes a temperature sensing refresh generator that senses the main memory temperature to issue a refresh frequency that increases or decreases in proportion with the sensed temperature. Pet. 23 (citing Ex. 1010, 24:15–23; Ex. 1005 ¶ 58). Further,

Petitioner asserts that Atkinson discloses an alternative embodiment with a voltage controller oscillator (VCO) combined with a temperature sensor, whereupon the VCO receives from the sensor a sensed temperature signal of the main memory, the VCO, produces in response a proportional refresh signal to refresh the main memory. *Id.* (citing Ex. 1010, 23:8–10, 23:17–20). We are persuaded by Petitioner's showing and find that Atkinson's description of the refresh generator teaches a refresh unit for providing to the DRAM an increased or decreased refresh rate in proportion with the sensed temperature of the DRAM. Likewise, we are persuaded that Atkinson's description of the VCO teaches a refresh timing unit to decrease the rate at which the DRAM array is refreshed as the signal indicates the temperature of the DRAM decreases.

2. Patent Owner's Assertions Regarding the References

As to the terms "refresh unit" and "refresh timing unit" recited in claims 6–11, Patent Owner argues the following:

(i) Petitioner fails to show that Atkinson teaches "'a refresh unit operable to refresh the DRAM array at a rate that varies in response to the signal'" (PO Resp. 58–59), and that

(ii) Petitioner fails to show Atkinson teaches "'a refresh timing unit operable to establish the rate at which the DRAM array is refreshed in response to the signal.'" *Id.* at 59–60.

We address each argument in turn.

i. The Allegation that Petitioner Fails to Show that Atkinson Teaches "a Refresh Unit Operable to Refresh the DRAM Array at a Rate that Varies in Response to the Signal"

Patent Owner argues that the statement in Atkinson relied upon by Petitioner teaches, at most, that the rate and the temperature are linked, but not that the rate "'varies in response to the signal.'" PO Resp. 58 (quoting Ex. 101, 24:15–23). According to Petitioner, the signal described in the statement is not equivalent to the signal recited in claim 6 because the signal described in Atkinson relates to a periodic voltage pulse produced by Atkinson's generator, whereas the claimed signal relates to a signal produced by the temperature sensor. *Id.* at 58–59. Accordingly, Patent Owner submits that Atkinson does not teach the required limitation of a signal indicative of the temperature of the DRAM array. *Id.* at 59.

This argument is not persuasive for the same reasons previously noted in our institution Decision. In particular, we noted the following:

> The antecedent basis for "the signal" is in claim 1, where Petitioner relies upon Atkinson's teaching of the refresh generator output, which is indicative of the temperature of the DRAM as measured by thermistor 800. Pet. 14–17 (discussing embodiments described in Figures 8 and 9 of Atkinson). In connection with the embodiment of Figure 8, Atkinson teaches explicitly that "[t]he frequency of the refresh signal in this embodiment continuously reduces as temperature decreases, rather than in discrete steps as in prior embodiments. Thus, refresh generator 850 provides a refresh signal that closely follows the temperature/frequency response of curve 600 or any other desired temperature/frequency response curve." Ex. 1010, 22:62–23:1. As a result, we agree with and are persuaded by Petitioner's contentions that Atkinson teaches refreshing the DRAM array at a rate that varies in response to the signal, as claim 6 requires, and not merely in response to the temperature of the DRAM array, as Patent Owner suggests.

Inst. Dec. 15–16.

We, therefore, reiterate our agreement with Petitioner that because Atkinson's refresh unit generates the refresh signal in response to receiving the DRAM temperature signal such that the generated refresh signal track the temperature signal proportionally, the generated refresh signal teaches the temperature signal. Reply 19–20.

On this record, Petitioner has shown by a preponderance of the evidence that Atkinson teaches "a refresh unit operable to refresh the DRAM array at a rate that varies in response to the signal."

ii. The Allegation that Petitioner Fails to Show Atkinson Teaches "'a Refresh Timing Unit Operable to Establish the Rate at Which the DRAM Array is Refreshed in Response to the Signal'"

Patent Owner argues Petitioner does not show that Atkinson's VCO is operable to establish the rate at which the DRAM array is refreshed in response to the sensed temperature signal. PO Resp. 59–60. According to Patent Owner, Atkinson's VCO merely 'produces a periodic waveform having a frequency that changes in response to changes in the input voltage. *Id.* at 60 (quoting Ex.1010, 23:5–9).

This argument is not persuasive. We agree with Petitioner that because Atkinson's VCO "'produces the refresh signal at the proper frequency'" in response to receiving a signal indicative of the temperature, the generated refresh signal sets the frequency to refresh the DRAM. Reply 21.

On this record, Petitioner has shown by a preponderance of the evidence that Atkinson teaches "'a refresh timing unit operable to establish the rate at which the DRAM array is refreshed in response to the signal.'"

d. Weight to be Given to Dr. Subramanian's Declaration

Patent Owner argues that no weight should be given to Dr. Subramanian's declaration because the declarant is not an attorney, he applied an incorrect legal test, and he is thereby not suited to provide opinions on the legal question of obviousness. PO Resp. 28–29. In support of this argument, Patent Owner directs attention to portions of Dr. Subramanian's deposition where he allegedly testified that background knowledge (including common sense) of an ordinary artisan can be routinely added to a combination to teach a missing limitation, even if the missing

limitation "'went to the heart of the invention.'" *Id.* at 29. According to Patent Owner, because the legal test allegedly applied by Dr. Subramanian was previously rejected by the Board's reviewing court in *Arendi S.A.R.L. v. Apple Inc.*, 832 F.3d 1355, 1361–65 (Fed. Cir. 2016) (2), the Board should disregard Dr. Subramanian's opinions on the ultimate question of obviousness. *Id.* at 29–30. Further, Patent Owner argues that Petitioner's declaration should be given little to no weight because the declaration allegedly parrots Petitioner's attorney's arguments. *Id.* at 30–31. According to Patent Owner, Petitioner's declaration section VII-B, for example, is exactly the same as Petition's section VII-B. *Id.* (citing Pet. 29–32; Ex. 1005, 28–30).

We have reviewed the arguments provided by Patent Owner and determine such arguments are insufficient to have Dr. Subramanian's declaration disregarded in its entirety. Rather, it is within our discretion to assign the appropriate weight to be accorded evidence. *See* 37 C.F.R. § 42.65(a); *see also, e.g.*, *Yorkey v. Diab*, 601 F.3d 1279, 1284 (Fed. Cir. 2010) (holding the Board has discretion to give more weight to one item of evidence over another "unless no reasonable trier of fact could have done so"); *In re Am. Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1368 (Fed. Cir. 2004) ("[T]he Board is entitled to weigh the declarations and conclude that the lack of factual corroboration warrants discounting the opinions expressed in the declarations."); *Velander v. Garner*, 348 F.3d 1359, 1371 (Fed. Cir. 2003) ("In giving more weight to prior publications than to subsequent conclusory statements by experts, the Board acted well within [its] discretion."). Based on the record before us, we are not persuaded that we should give the entirety of Dr. Subramanian's declaration no weight. We reiterate

nonetheless that we reached the ultimate conclusion of obviousness in this Decision based on the totality of the record before us, and without adopting any purported "lay opinions".[8]

e. Summary

For the foregoing reasons, we are persuaded that Petitioner has established, by a preponderance of the evidence the following:

(1) Claims 1, 3, 5–9, 12, 13, and 16 of the '057 patent are unpatentable under 35 U.S.C. § 103(a) over the combination of Atkinson and Broadwater;

(2) Claims 2, 4, 10, 11, 14, 15, and 17 of the '057 patent are unpatentable under 35 U.S.C. § 103(a) over the combination of Atkinson, Broadwater, and Miller.

III. CONCLUSION

Petitioner has demonstrated, by a preponderance of the evidence, that: (1) Claims 1, 3, 5–9, 12, 13, and 16 of the '057 patent are unpatentable under 35 U.S.C. § 103(a) over the combination of Atkinson and Broadwater; (2) Claims 2, 4, 10, 11, 14, 15, and 17 of the '057 patent are unpatentable under 35 U.S.C. § 103(a) over the combination of Atkinson, Broadwater, and Miller.

[8] See supra note 5.

IV. ORDER

Accordingly, it is

ORDERED that claims 1–17 of the '057 patent are determined to be *unpatentable*;

FURTHER ORDERED that, because this is a Final Written Decision, parties to the proceeding seeking judicial review of the decision must comply with the notice and service requirements of 37 C.F.R. § 90.2.

IPR2016-01621
Patent 6,438,057 B1

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ATTACHMENT 2

Kenneth Weatherwax

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Subject: RE: IPR2016-01621/1622/1623

Counsel,

The panel has determined that a call is not necessary, and will issue an Order addressing Patent Owner's request.

Regards,

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Subject: IPR2016-01621/1622/1623

To the Honorable Board:

Pursuant to 35 U.S.C. § 316(a)(13) and 37 C.F.R. § 42.23(b), Patent Owner requests a call with the Board in the above-referenced co-scheduled proceedings for guidance on how to address the scope of Petitioner's reply submissions that are in Patent Owner's view new and outside the scope of proper reply.

Patent Owner earnestly seeks the Board's guidance on this question in light of the varying approaches Board panels in other cases have taken as to how, and when, this issue is properly to be raised by the patent owner.

Petitioner has not taken a position at this time on the merits of this request. I am authorized to state that Petitioner counsel is available for a call at Thursday from 11-1pm ET and 2:30-5 ET. Patent Owner is available at those times as well.

Respectfully submitted,

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Paper 8
Entered: February 15, 2017

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KINGSTON TECHNOLOGY COMPANY, INC.,
Petitioner,
v.

POLARIS INNOVATIONS LTD.,
Patent Owner.

Case IPR2016-01621
Patent 6,438,057 B1

Before SALLY C. MEDLEY, JEAN R. HOMERE, and MATTHEW R. CLEMENTS, *Administrative Patent Judges*.

HOMERE, *Administrative Patent Judge*.

DECISION
Granting Institution of *Inter Partes* Review
37 C.F.R. § 42.108

I. INTRODUCTION

Kingston Technology Company, Inc. ("Petitioner") filed a Petition for *inter partes* review of claims 1–17 of U.S. Patent No. 6,438,057 B1 (Ex. 1001, "the '057 patent"). Paper 3 ("Pet."). Polaris Innovations Ltd. ("Patent Owner") filed a Preliminary Response. Paper 8 ("Prelim. Resp."). Institution of an *inter partes* review is authorized by statute when "the information presented in the petition . . . and any response . . . shows that there is a reasonable likelihood that the petitioner would prevail with respect to at least 1 of the claims challenged in the petition." 35 U.S.C. § 314(a); *see* 37 C.F.R. § 42.108.

Upon consideration of the Petition and Preliminary Response, we conclude the information presented shows there is a reasonable likelihood that Petitioner would prevail in establishing the unpatentability of claims 1–17 of the '057 patent.

A. Related Matters

The parties state that the '057 patent is the subject of a pending lawsuit in the Central District of California Southern Division that includes assertions against Petitioner. Pet. 2; Paper 5 (Patent Owner's Mandatory Notice), 1; Ex. 1002.

B. The '057 Patent

The '057 patent is directed to a method and system for refreshing the contents of a dynamic random access memory (DRAM) array. Ex. 1001, 1:5–7. In particular, the temperature of the DRAM array is utilized to adjust

a refresh rate at which the contents of the DRAM array are updated. *Id*. at 1:7–10. Figure 3 of the '057 patent is reproduced below:

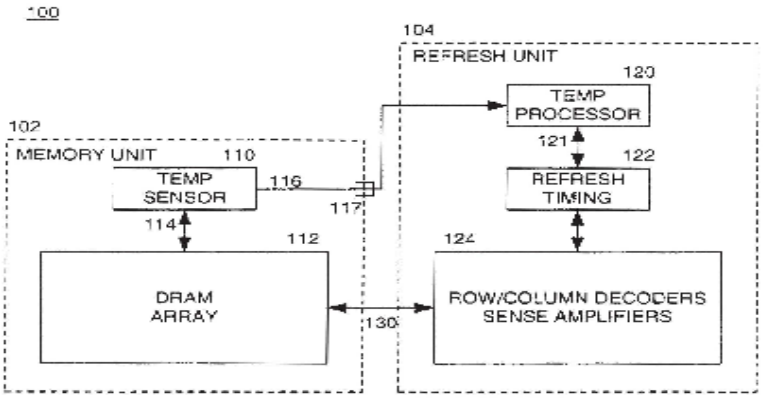

FIG. 3

Figure 3 illustrates system 100 for storing data in DRAM array 112. *Id*. at 4:11–12. In particular, Figure 3 depicts memory unit 102 containing temperature sensor 110 coupled to DRAM array 112, wherein memory unit 102 is connected to refresh unit 104 containing temperature processor 120 coupled to refresh timing 122 and row/column decoders sense amplifiers 124. *Id*. at 4:12–30. According to the '057 patent, "the DRAM array 112 may be implemented on a semiconductor chip and the temperature sensor 110 may be thermally coupled to the same semiconductor chip or to an intermediate member that is in thermal communication with the semiconductor chip." *Id*. at 4:22–26.

More specifically, in system 100 illustrated in Figure 3, upon receiving signal 116 from temperature sensor 110 indicating a temperature sensed from DRAM array 112, refresh unit 104 produces refresh signal 130 to refresh DRAM array 112 at a rate that varies in response to received temperature signal 116. *Id*. at 4:30–32. Preferably, DRAM array 112 is

refreshed at a rate that decreases as the temperature of DRAM array 112 decreases. Conversely, DRAM array 112 is refreshed at a rate that increases as the temperature of DRAM array 112 increases. *Id*. at 4:33–37. Further, according to the '057 patent, "the temperature sensor 110 and the DRAM array 112 are preferably disposed in a semiconductor package where the package includes at least one connection pin 117 operable to provide the signal on line 116 to external circuitry, such as the refresh unit 104." *Id*. at 4:49–53. "[T]he temperature sensor 110 preferably includes at least one diode 140 having a forward voltage drop that varies as a function of the temperature of the DRAM array 112." Ex. 1001 at 5:17–20.

C. Illustrative Claim

Petitioner challenges claims 1–17 of the '057 patent. Pet. 9. Claims 1, 13, and 16 are independent claims. Claims 2–12 depend either directly or indirectly from claim 1. Claims 14 and 15 depend either directly or indirectly from claim 13. Claim 17 depends from claim 16. *Id*. at 5:60–8:13.

Independent claim 1, reproduced below, is illustrative of the claimed subject matter:

> 1. An apparatus, comprising:
>
> a semiconductor package including at least one connection pin;
>
> at least one dynamic random access memory (DRAM) array disposed within the package; and
>
> at least one temperature sensor in thermal communication with the DRAM array, operable to produce a signal indicative of a temperature of the DRAM array, and coupled to the at least

> one connection pin such that the signal may be provided to external circuitry,
>
> wherein the DRAM array is refreshed at a rate that decreases as the temperature of the DRAM array decreases and that increases as the temperature of the DRAM array increases.

Id. at 5:60–6:7.

Independent claim 13 is similar to claim 1, except that it includes a DRAM chipset comprising a "DRAM chip including a DRAM array and at least a temperature sensor" and one "refresh chip operable to refresh the DRAM array." *Id*. at 6:59–7:6. Independent claim 16 is similar to claim 1, except that it sets forth a method for refreshing contents of a DRAM array at a rate that varies proportionally in response to temperature increases/decreases of the DRAM array. *Id*. at 8:1–9.

D. Asserted Grounds of Unpatentability

Petitioner asserts that claims 1–17 are unpatentable based on the following grounds (Pet. 9–10):

Reference(s)	**Basis**	**Challenged Claims**
Atkinson[1]	§ 103(a)	1–17
Atkinson and Broadwater et al.[2]	§ 103(a)	1, 3, 5–9, 12, 13, and 16
Atkinson, Broadwater, and Miller et al.[3,4]	§ 103(a)	2, 4, 10, 11, 14, 15, and 17

[1] US 6,134,167, issued Oct. 17, 2000 (Ex. 1010) ("Atkinson").
[2] US 4,970,497, issued Nov. 13, 1990 (Ex. 1006) ("Broadwater").
[3] US 3,812,717, issued May 28, 1974 (Ex. 1015) ("Miller").
[4] Although Miller is omitted from Petitioner's summary of asserted grounds, it is nevertheless relied upon in Petitioner's analysis of claims 2, 4, 10, 11, 14, 15, and 17. *See, e.g.*, Pet. 20. We, therefore, treat Petitioner's analysis of claims 2, 4, 10, 11, 14, 15, and 17 based upon Atkinson, Broadwater, and Miller from the statement as a separate ground of unpatentability.

Reference(s)	Basis	Challenged Claims
Tillinghast et al.[5] and Broadwater	§ 103(a)	1–17
Kodama[6] and Lee et al.[7] or Broadwater	§ 103(a)	1–17

II. DISCUSSION

A. Claim Construction

In an *inter partes* review, we construe claim terms in an unexpired patent according to their broadest reasonable construction in light of the specification of the patent in which they appear. 37 C.F.R. § 42.100(b).

Consistent with the broadest reasonable construction, claim terms are presumed to have their ordinary and customary meaning as understood by a person of ordinary skill in the art in the context of the entire patent disclosure. *In re Translogic Tech., Inc*., 504 F.3d 1249, 1257 (Fed. Cir. 2007).

Patent Owner contends that because Petitioner has not provided in the Petition how each of the challenged claims is to be construed, but instead advises the Board that the claims are to be construed according to their broadest reasonable interpretation, Petitioner has failed to demonstrate a scope of the claimed invention that permits the Board to apply the asserted references to the claims. Prelim. Resp. 5, 8. Further, Patent Owner contends that because Petitioner previously argued in the companion district court litigation that eight different claim terms are indefinite and cannot be construed, Petitioner cannot now request the Board to construe those claim terms according to their broadest reasonable interpretation ("BRI"). *Id*. at 5–

[5] US 5,278,796, issued Jan. 11, 1994 (Ex. 1009) ("Tillinghast").
[6] US 3,851,316, issued Nov. 26, 1974 (Ex. 1004) ("Kodama").
[7] US 5,229,970, issued July 20, 1993 (Ex. 1011) ("Lee").

7. Patent Owner therefore submits that Petitioner has failed to meet its burden to demonstrate, with reasonable certainty, the scope of the claims to which the Board is to apply the alleged prior art. *Id*. at 7–9.

As set forth above and as correctly noted by the parties, we construe claim terms in an unexpired patent according to the broadest reasonable interpretation. Pet. 11 (citing *Cuozzo Speed Techs. LLC v. Lee*, 136 S. Ct. 2131, 2142–46 (2016); Prelim. Resp. 8. Neither party argues that a claim term is indefinite, and we are not persuaded by Patent Owner's reference to Petitioner's prior allegation of indefiniteness of certain claim terms in the district court proceeding that any of those terms are indefinite. Further, neither party proffers a construction of, or otherwise disputes the meaning of, any of the claim terms. We determine, at this juncture of the proceeding, that it is not necessary to provide any express interpretation of the claim terms. Only terms that are in controversy need to be construed, and then only to the extent necessary to resolve the controversy. *Vivid Techs., Inc. v. Am. Sci. & Eng'g, Inc.*, 200 F.3d 795, 803 (Fed. Cir. 1999).

B. Asserted Obviousness over Atkinson and Broadwater

Petitioner contends claims 1, 3, 5–9, 12, 13, and 16 are unpatentable under 35 U.S.C. § 103(a) over the combination of Atkinson and Broadwater. Pet. 29–32 (referencing *id*. at 12–28). Relying on the declaration of Dr. Vivek Subramanian, Petitioner explains how the proposed combination of references discloses all of the claim limitations. *Id*. at 12–19, 23–32 (citing Ex. 1005).

1. Atkinson

Atkinson describes a technique for reducing the consumption of electric power in the main computer memory. Ex. 1010, 1:16–20. In particular, Atkinson discloses a refresh logic device that generates a memory refresh signal having a rate, which varies proportionally with the sensed temperature of the computer memory. *Id*. at 5:61–66, 7:41–44.

Figure 8 of Atkinson is reproduced below.

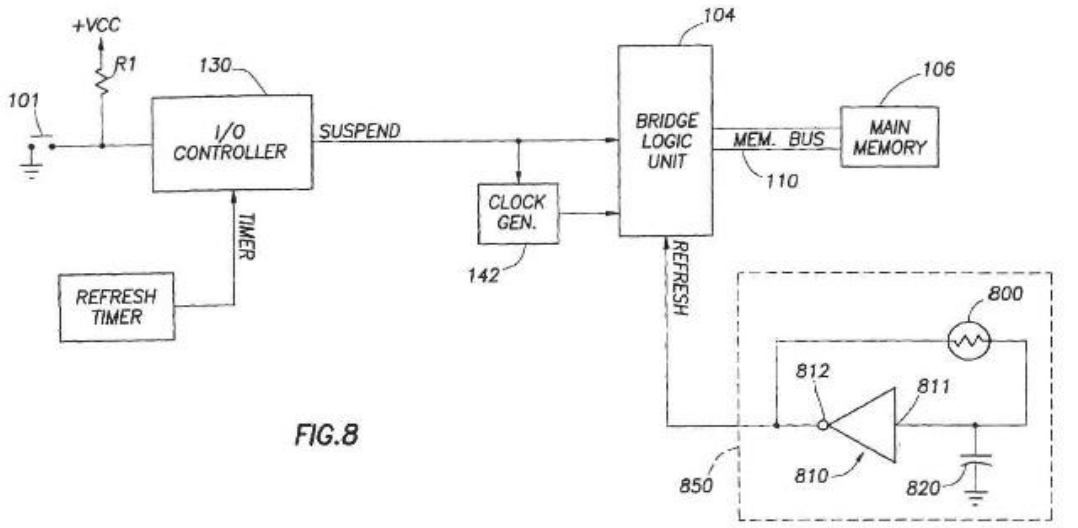

FIG.8

As illustrated in Figure 8 of Atkinson, refresh generator 850 includes thermistor 800, the temperature of which drops upon sensing a decreased temperature of main memory 106 to thereby produce a decrease of the rate of the refresh signal. *Id*. at 22:39–65. "Accordingly, the refresh temperature of the thermistor 800 represents the temperature of the memory storage logic 930, and the refresh frequency decreases approximately in proportion to the decrease in the temperature of the memory storage logic 930." *Id*. at 24:11–17. Conversely, when the temperature of thermistor 800 increases upon sensing an increased temperature of main memory 106, refresh generator 850 increases the rate of the refresh signal. *Id*. at 7:41–44, 21:38–39.

Atkinson also discloses an alternative embodiment in which refresh generator 950, including thermistor 800, is integrated in main memory 906. *Id*. at 23:37–40, 24:11–13, 24:22–23, Fig. 9.

Atkinson further discloses that that main memory 906 is an alternative embodiment of main memory 106 that preferably comprises DRAM circuitry (*id.* at 23:32–34), but may also be other types of DRAM, such as synchronous DRAM (SDRAM), extended data output DRAM (EDO RAM), and Rambus RAM. *Id*. at 3:38–46, 9:1–5. Main memory 106 is connected to bus 110 to exchange signals therewith. *Id*. at 12:4–7.

2. Broadwater

Broadwater relates to a technique for sensing and reducing the effects of thermal stress on packaged semiconductor chips. Ex. 1006, 1:6–8, Abstract. Figure 1 of Broadwater is reproduced below:

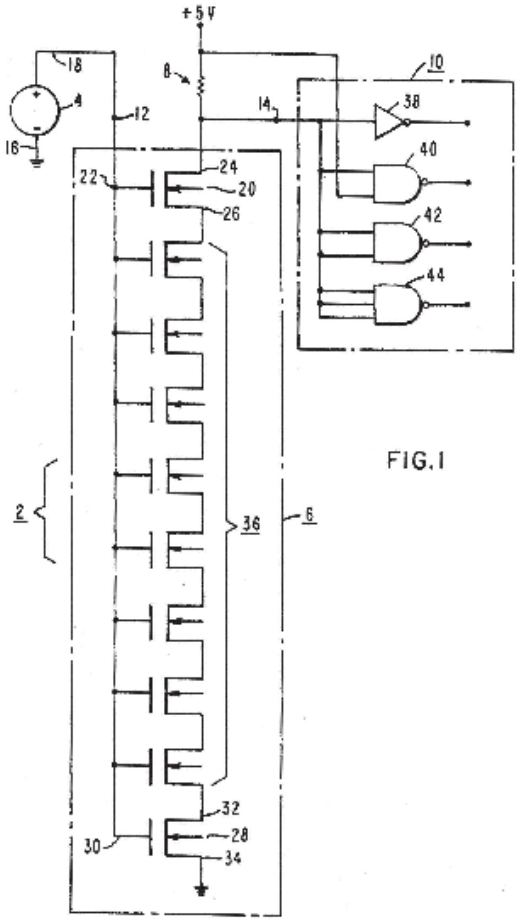

FIG. 1

As depicted in Figure 1 above, Broadwater describes a chip package having thermal stress sensing circuit 6 with input 12 and output 14. *Id.* at 4:3:31–35. The voltage at output 14 varies as a function of input voltage and temperature. *Id.* at 4:39–41, Fig. 2. Output 14 can be routed to gate array 10, as shown, or can be provided to an external pin of the chip package. *Id.* at 4:31–53.

3. Discussion

Petitioner asserts that the combination of Atkinson and Broadwater discloses the elements of claims 1, 3, 5–9, 12, 13, and 16. Pet. 12–32. We begin our analysis with claim 1. The preamble of claim 1 recites "an apparatus comprising." Ex. 1001, 5:61. Petitioner contends that Atkinson's

description of an apparatus containing a main memory with a temperature sensor discloses the preamble of claim 1. Pet. 12.

Claim 1 next recites "a semiconductor package including at least one connection pin." Ex. 1001, 5:62–63. Petitioner contends that Atkinson's description of main memory 106 including any suitable type of memory such as DRAM or any of the special types of DRAM devices (e.g., SDRAM, EDO DRAM, Rambus DRAM) discloses the "semiconductor package" because "one of ordinary skill in the art would know that SDRAM and Rambus DRAM are packaged semiconductor chips." Pet. 13 (citing Ex. 1005 ¶ 41; Ex. 1007, 524; Ex. 1010, 4:31–35, 8:65–9:5). Further, Petitioner asserts that Atkinson's description of main memory 106's connection to bus 110 discloses the "connection pin" because one of ordinary skill would appreciate that "as the main memory is composed of packaged memory chips that receive a variety of bus signals," its "connections to the memory bus 110 would necessarily require at least one connection pin or it would be obvious to have one." *Id*. at 13–14 (citing Ex. 1010, 12:4–7, 23:32–37, 12:8–12; Ex. 1005 ¶ 42).

Claim 1 also recites "at least one dynamic random access memory (DRAM) array disposed within the package." Ex. 1001, 5:64–65. Petitioner asserts that Atkinson's description of a "computer system where the main memory 106 includes an array of memory devices such as DRAM" discloses the "package" having disposed therein the DRAM array. Pet. 14 (citing Ex. 1010, Figs. 1, 4A, 5, 7–9, 5:57–62, 8:37–9:15; Ex. 1005 ¶ 43).

Claim 1 further recites "at least one temperature sensor in thermal communication with the DRAM array, operable to produce a signal indicative of a temperature of the DRAM array." Ex. 1001, 5:66–6:1.

Petitioner asserts Atkinson's description of refresh generator 850, including thermistor 800 that directly senses the temperature of the DRAM, discloses "the temperature sensor . . . in thermal communication with the DRAM array." Pet. 14–16 (citing Ex. 1010, 22:52–62, 22:39–67, 23:32–37, 24:1–26, Fig. 8; Ex. 1005 ¶¶ 44, 45). Further, Petitioner asserts Atkinson describes an alternate embodiment wherein a "voltage controlled oscillator [(VCO)] combined with the temperature sensor could replace the refresh generator," such that "the temperature sensor couples to main memory 106, providing a voltage to the VCO that represents the main memory temperature." Pet. 16 (citing Ex. 1010, 23:5–19). The refresh signal produced by the VCO varies with the temperature of the memory device as sensed by the temperature sensor. Pet. 16–17 (citing Ex. 1010, 6:46–62, 7:46–48).

Claim 1 also recites "coupled to the at least one connection pin such that the signal may be provided to external circuitry." Ex. 1001, 6:2–3. Petitioner asserts that Atkinson describes an on-chip embodiment wherein a temperature sensor coupled directly to main memory 106 provides a voltage to the VCO that represents the main memory temperature. Pet. 17 (citing Ex. 1010, 23:15–17, Fig. 8; Ex. 1005 ¶ 47). According to Petitioner, while the on-chip embodiment described by Atkinson does not disclose providing the temperature signal to an external circuit, such a modification would have been obvious to one of ordinary skill in the art, particularly in view of Broadwater's disclosure of an external pin of a chip package (e.g., DRAM memory chip) for outputting a signal indicative of the chip's temperature. *Id*. (citing Ex. 1005 ¶¶ 47–49); *id*. at 30 (citing Ex. 1006, 4:31–33, 4:49–53; Ex. 1005 ¶¶ 83–84). Further, Petitioner asserts that the ordinarily skilled

artisan would have been motivated to combine the cited disclosures of Atkinson and Broadwater because Broadwater's disclosure of adding an external pin to an existing chip package (e.g., Atkinson's DRAM) would help reduce the effects of thermal stress on the DRAM. *Id*. at 31 (citing Ex. 1006, 1:14–29; Ex. 1005 ¶ 85). Additionally, Petitioner concludes that the ordinarily skilled artisan would have recognized that the proposed combination would help maximize power saving during the self-refresh timing sequence. *Id*. (citing Ex 1005 ¶ 86).

Claim 1 also recites "wherein the DRAM array is refreshed at a rate that decreases as the temperature of the DRAM array decreases and that increases as the temperature of the DRAM array increases." Ex. 1001, 4:4–7. Petitioner asserts Atkinson describes a refresh logic that reduces the rate of the refresh signal in response to receiving a signal from the temperature sensor indicating a drop in the main memory temperature. Pet. 19 (citing Ex. 1010, 13:13–15, 22:2–7). Conversely, the refresh logic increases the rate of the refresh signal in response to receiving a signal indicating an increase in the temperature of the main memory. *Id*. (citing 1010, 7:41–44; Ex. 1005 ¶¶ 50–51). According to Petitioner, the refresh frequency increases or decreases in proportion to the increase or decrease in the temperature of the DRAM as a way to achieve the greatest power savings. *Id*. (citing Ex. 1010, 20:53–56, 24:3–17, Fig. 6; Ex. 1005 ¶ 51).

Independent claims 13 and 16 are similar to claim 1. Petitioner has made a showing with respect to claims 13 and 16 similar to its showing with respect to claim 1. *See, e.g.*, Pet. 26–28. To the extent that claims 13 and 16 are different from claim 1, Petitioner has accounted for such differences.

We also have reviewed Petitioner's showing with respect to dependent claims 3, 5–9, and 12. *Id*. at 21, 23–26.

Patent Owner argues that Petitioner has not accounted sufficiently for each limitation and has not articulated sufficiently a reason to combine the prior art references. Prelim. Resp. 12–34. We address each argument in turn.

Patent Owner contends that Petitioner does not identify in Atkinson a semiconductor package including a "connection pin," as required by independent claims 1 and 13. *Id*. at 13. This argument is not persuasive. As discussed above, Petitioner reasoned that "[a]s the main memory is composed of packaged memory chips that receive a variety of memory bus signals, one of ordinary skill in the art would appreciate that connections to the memory bus 110 would necessarily require at least one connection pin, or it would be obvious to have one." Pet. 13–14 (citing Ex 1005 ¶¶ 41, 42). Further, at this stage of the proceeding, Dr. Subramanian's testimony is unrebutted. For the foregoing reasons, we agree, on this record, with Petitioner's reasoning.

Patent Owner contends similarly that Petitioner does not demonstrate that the Atkinson-Broadwater combination includes a connection pin that provides a signal to external circuitry. Prelim. Resp. 31–32. As just discussed, however, we are persuaded, on this record, by Petitioner's argument that the limitation of providing the temperature signal to an external circuit is taught by the proposed combination of Atkinson's on-chip embodiment with Broadwater's an external pin of a chip package (e.g., DRAM memory chip) for outputting a signal indicative of the chip's temperature. Pet. 30.

Further, Patent Owner argues that Petitioner does not provide a motivation to combine Atkinson with Broadwater. *Id*. at 32–34. This argument is unavailing. Petitioner asserts the ordinarily skilled artisan would be motivated to combine the cited disclosures of Atkinson and Broadwater because Broadwater's disclosure of adding an external pin to Atkinson's DRAM would help reduce the effects of thermal stress on the DRAM, and would help maximize power saving during the self-refresh timing sequence. *Id*. at 31 (citing Ex. 1005 ¶¶ 85, 86). At this stage, moreover, Dr. Subramanian's testimony is unrebutted. We are persuaded, on this record, that Petitioner has provided an articulated reasoning with some rational underpinning sufficient to support the legal conclusion of obviousness. *KSR Int'l Co. v. Teleflex Inc.*, 550 U.S. 398, 418 (2007) (citing *In re Kahn*, 441 F.3d 977, 988 (Fed. Cir. 2006)).

Patent Owner also argues that "Petitioner does not provide evidence dictating that the rate 'varies in response to the *signal*,' as [claim 6] requires." Prelim. Resp. 23–26. In particular, Patent Owner argues that the cited portion of Atkinson "may well demonstrate that the rate and the temperature are linked," but does not teach "that it is *the signal* that causes the rate to decrease in proportion to the decrease in temperature." *Id.* at 23 (emphasis added). This argument is not persuasive. The antecedent basis for "the signal" is in claim 1, where Petitioner relies upon Atkinson's teaching of the refresh generator output, which is indicative of the temperature of the DRAM as measured by thermistor 800. Pet. 14–17 (discussing embodiments described in Figures 8 and 9 of Atkinson). In connection with the embodiment of Figure 8, Atkinson teaches explicitly that "[t]he frequency of the refresh signal in this embodiment continuously

reduces as temperature decreases, rather than in discrete steps as in prior embodiments. Thus, refresh generator 850 provides a refresh signal that closely follows the temperature/frequency response of curve 600 or any other desired temperature/frequency response curve." Ex. 1010, 22:62–23:1. As a result, we agree with and are persuaded by Petitioner's contentions that Atkinson teaches refreshing the DRAM array at a rate that varies in response to the *signal*, as claim 6 requires, and not merely in response to the temperature of the DRAM array, as Patent Owner suggests.

Patent Owner also argues that Petitioner's contentions with respect to claim 7 are inconsistent with positions taken by Petitioner in the corresponding district court litigation. Prelim. Resp. 26–27. This argument is not persuasive. As noted above, neither party argues in this proceeding that the term "refresh unit" recited in claim 7 is a means-plus-function term or that it is indefinite. Consequently, Patent Owner's reference to Petitioner's prior construction of "refresh unit" in the district court proceeding is not persuasive. On this record, we are persuaded that Atkinson's voltage controller oscillator (VCO) describes the refresh timing unit. Pet. 23–24.

Patent Owner also argues that Petitioner's contentions with respect to claims 8 and 9 rely on two distinct embodiments of Atkinson without explaining "how or why one would combine the two embodiments." Prelim. Resp. 28. This argument is not persuasive. Although Atkinson describes a first embodiment including refresh generator 850, and another embodiment wherein the refresh generator is replaced with the VCO combined with a temperature sensor, Petitioner does not rely upon the two cited embodiments to describe the limitations claims 8 and 9. Instead, Petitioner relies only

upon the latter embodiment to meet the claim limitations. *See* Pet. 24–25. Even if Petitioner relied upon both embodiments to support the assertion of obviousness, such a combination would not necessarily be improper because this ground is based upon obviousness rather than anticipation.

Finally, with respect to claim 13, Patent Owner argues that Petitioner has not identified with sufficient clarity what in Atkinson teaches the recited "DRAM chip," "refresh chip," "connection pin," or "external circuitry." Prelim. Resp. 29–30. We disagree. As noted above, Petitioner has made a showing with respect to claim 13 similar to its showing with respect to claim 1. *See, e.g.*, Pet. 26–28. To the extent that claim 13 is different from claim 1, Petitioner has accounted for such differences. *Id*.

Based on the current record before us, we determine that there is a reasonable likelihood that Petitioner would prevail in establishing that claims 1, 3, 5–9, 12, 13, and 16 are unpatentable over the combination of Atkinson and Broadwater.

C. Asserted Obviousness over Atkinson, Broadwater, and Miller

Petitioner contends claims 2, 4, 10, 11, 14, 15, and 17 are unpatentable under 35 U.S.C. § 103(a) as obvious over the combination of Atkinson, Broadwater, and Miller.[8] Pet. 20–21, 22, 25, 27, 28, and 29–30. Relying on the declaration of Dr. Subramanian, Petitioner explains how the proposed combination of references discloses all of the claim limitations. *Id*. (citing Ex. 1005).

[8] *See supra* note 4.

On this record, Petitioner has accounted sufficiently for the limitations of claims 2, 4, 10, 11, 14, 15, and 17. For example, claim 2 depends directly from claim 1 and recites "wherein the at least one temperature sensor includes at least one diode having a forward voltage drop that varies as a function of the temperature of the DRAM array, and the signal corresponds to the forward voltage drop of the at least one diode." Ex. 1001, 6:8–12.

Petitioner asserts that, although the '057 patent includes a diode as a known temperature sensor, it also discloses other known temperature sensors (e.g., thermocouples, thermistors, or any other device that provides an output signal varying as a function of temperature). Pet. 20 (citing Ex. 1001, 2:42–45). Petitioner further asserts that Atkinson similarly discloses the use of such known temperature sensors (e.g., thermocouple or temperature sensing integrated circuit). *Id*. (citing Ex. 1010, 22:21–24; Ex. 1005 ¶¶ 52, 53). Petitioner then contends that, at the time of the invention, measuring a forward voltage drop across a semiconductor diode to thereby read the temperature, as described in Miller, was a well-known use of such a type of temperature sensor. Pet. 20 (citing Ex. 1015, Abstract). Petitioner concludes it would have been obvious to one of ordinary skill in the art to select a diode as a well-known type of temperature sensor for reading the temperature of Atkinson's DRAM. *Id*. at 21 (citing Ex. 1010, 24:63–65; 1005 ¶ 53).

Likewise, claim 4 depends directly from claim 1, and recites

> wherein the at least one temperature sensor includes having a forward voltage drop that varies as a function of the temperature of the DRAM array; the at least one connection pin includes a first pin coupled to an anode of the diode and a second pin coupled to the cathode of the diode; and the signal corresponds to a potential voltage between the first and second pins.

Ex. 1001, 6:17–23.

Petitioner explains, with supporting evidence, that at the time of the invention, "given that the claim merely recites 'first pin' and 'second pin,' the diode temperature sensor would necessarily be connected to a first pin and a second pin if it were operational." *Id*. at 22 (citing Ex. 1005 ¶ 56). Petitioner further explains that "in such a diode configuration, the signal between the first pin and the second pin would necessarily be the forward voltage drop of the diode, which claim 4 defines as the signal." *Id*. Petitioner concludes that it would have been obvious to one of ordinary skill in the art at the time of the invention to "modify Atkinson to use a diode configuration as recited in claim 4 (which is essentially the same as the obvious variant in claim 2)." *Id*.

We also have reviewed the Petition with respect to dependent claims 10, 11, 14, 15, and 17, and determine that at this juncture of the proceeding Petitioner has accounted sufficiently for the recited limitations. Pet. 25, 27 and 28.

Patent Owner argues that Petitioner's reliance on "finite alternate types of integrated circuits for detecting temperatures" is a misapplication of *KSR* because the number of available alternatives is "far from 'small or easily traversed.'" Prelim. Resp. 19–23(citing *Ortho-McNeill Pharmaceutical, Inc., v. Mylan Laboratories,, Inc.*, 520 F.3d 1358, 1364 (Fed. Cir. 2008). This argument is moot in light of Petitioner's alternative reliance upon Miller's diode to measure the temperature of Atkinson's DRAM. Pet. 20.

Patent Owner also argues that Miller is not part of any combination and that no motivation is given by Petitioner to combine Atkinson with

Miller. Prelim. Resp. 22. As discussed above, however, we interpret the ground of unpatentability as including Miller.[9] Petitioner has sufficiently shown, at this stage of the proceeding, that it would have been obvious to use the diode described in Miller to read and measure the temperature of Atkinson's DRAM. Pet. 20–21. On the record before us, we are persuaded that Petitioner has provided an articulated reasoning with some rational underpinning sufficient to support the legal conclusion of obviousness based on Atkinson, Broadwater, and Miller. *See KSR*, 550 U.S. at 418.

For the foregoing reasons, we determine the information presented shows a reasonable likelihood that Petitioner would prevail in establishing that the subject matter of claims 2, 4, 10, 11, 14, 15, and 17 would have been obvious over the combination of Atkinson, Broadwater, and Miller.

D. Remaining Grounds

Petitioner argues that the challenged claims are unpatentable under 35 U.S.C. § 103 as obvious over (1) Atkinson alone; (2) Tillinghast and Broadwater; and (3) Kodama and Lee '970 or Broadwater. Pet. 12–28, 33–61. The Board's rules for AIA *inter partes* proceedings, including those pertaining to institution, are "construed to secure the just, speedy, and inexpensive resolution of every proceeding." 37 C.F.R. § 42.1(b); *accord* 35 U.S.C. §§ 316(b) (regulations for AIA *inter partes* proceedings take into account "the efficient administration of the Office" and "the ability of the Office to timely complete [instituted] proceedings"). Because we institute an *inter partes* review of these claims based on the grounds discussed above, we exercise our discretion not to institute a review based on these grounds

[9] *See supra* notes 3 & 4.

for reasons of administrative expediency to ensure timely completion of the instituted proceeding. *See* 37 C.F.R. § 42.108(a) ("the Board may authorize the review to proceed . . . on all or some of the grounds of unpatentability asserted for each claim"); 35 U.S.C. § 314(a) (authorizing institution of an *inter partes* review under particular circumstances, but not requiring institution under any circumstances); *Harmonic Inc. v. Avid Tech., Inc.*, 815 F.3d 1356, 1368 (Fed. Cir. 2016) ("[U]nder [37 C.F.R. § 42.108(a)], it is clear that the Board may choose to institute some grounds and not institute others as part of its comprehensive institution decision.").

III. CONCLUSION

For the foregoing reasons, we determine that the information presented establishes a reasonable likelihood that Petitioner would prevail in showing that claims 1–17 of the '057 patent are unpatentable. At this preliminary stage, we have not made a final determination with respect to the patentability of the challenged claims or any underlying factual or legal issues.

IV. ORDER

ORDERED that pursuant to 35 U.S.C. § 314(a), an *inter partes* review is hereby instituted as to claims 1–17 of the '057 patent on the following grounds of unpatentability:

References	**Basis**	**Challenged Claims**
Atkinson and Broadwater	§ 103(a)	1, 3, 5–9, 12, 13, and 16
Atkinson, Broadwater, and Miller	§ 103(a)	2, 4, 10, 11, 14, 15, and 17

FURTHER ORDERED that pursuant to 35 U.S.C. § 314(c) and 37 C.F.R. § 42.4, notice is hereby given of the institution of a trial commencing on the entry date of this decision; and

FURTHER ORDERED that the trial is limited to the grounds identified immediately above, and no other ground is authorized.

IPR2016-01621
Patent 6,438,057 B1

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Paper No. 22
Entered: August 30, 2017

UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

KINGSTON TECHNOLOGY COMPANY, INC.,
Petitioner,

v.

POLARIS INNOVATIONS LTD.,
Patent Owner.

IPR2016-01621 (Patent 6,438,057 B1)
IPR2016-01622 (Patent 6,850,414 B2)
IPR2016-01623 (Patent 7,315,454 B2)[1]

Before SALLY C. MEDLEY, JEAN R. HOMERE, and MATTHEW R. CLEMENTS, *Administrative Patent Judges*.

CLEMENTS, *Administrative Patent Judge*.

ORDER
Conduct of the Proceedings
37 C.F.R. § 42.5

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[1] This Order addresses issues identical in all three cases. We, therefore, exercise our discretion to issue one Order to be filed in each case. The parties are not authorized to use this style heading for any subsequent papers

IPR2016-01621 (Patent 6,438,057 B1)
IPR2016-01622 (Patent 6,850,414 B2)
IPR2016-01623 (Patent 7,315,454 B2)

On August 29, 2017, counsel for Polaris Innovations Ltd. ("Patent Owner") requested a conference call to seek the panel's guidance on how to address portions of each Reply filed by Kingston Technology Company Inc. ("Petitioner") that, in its view, are outside the proper scope of a reply.

We will determine whether the allegedly new arguments and evidence are outside the proper scope of a reply in the final written decision. To preserve the issue in the words of the parties, we authorize Patent Owner to file, in each proceeding, a brief paper, limited to two pages, that only identifies the new and improper arguments and evidence introduced in Petitioner's Reply, generally by exhibit, page, and/or line number(s) only, and does not present any arguments. Petitioner is authorized to file, in each proceeding, a brief response, limited to two pages, that identifies the portions of the Patent Owner Response to which the new arguments and evidence identified by Patent Owner are a proper response or that identifies where this argument or evidence is presented in the Petition, also generally by exhibit, page, and/or line number(s) only. The deadlines for the respective papers are set forth below.

Either party may bring up the subject at the time of oral hearing. However, our guidance at oral hearings will be the same—if we determine Petitioner's arguments or evidence are outside the proper scope of a reply, we will not consider those arguments or evidence, and if we determine that Petitioner's arguments and evidence is responsive to the Patent Owner Response, we will consider Petitioner's arguments and evidence.

IPR2016-01621 (Patent 6,438,057 B1)
IPR2016-01622 (Patent 6,850,414 B2)
IPR2016-01623 (Patent 7,315,454 B2)

ORDER

Accordingly, it is

ORDERED that Patent Owner is authorized to file, in each proceeding, on or before September 6, 2017, a paper not exceeding two pages to identify the new arguments and evidence relied upon in Petitioner's Reply that it believes to be beyond the proper scope of a reply; and

FURTHER ORDERED that Petitioner is authorized to file, in each proceeding, on or before September 13, 2017, a paper not exceeding two pages to identify either the portions of the Patent Owner Response to which the new arguments and evidence identified by Patent Owner is a proper response, or the portions of the Petition where the arguments and evidence were made initially.

IPR2016-01621 (Patent 6,438,057 B1)
IPR2016-01622 (Patent 6,850,414 B2)
IPR2016-01623 (Patent 7,315,454 B2)

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US006438057B1

(12) **United States Patent**
Ruckerbauer

(10) **Patent No.: US 6,438,057 B1**
(45) **Date of Patent: Aug. 20, 2002**

(54) **DRAM REFRESH TIMING ADJUSTMENT DEVICE, SYSTEM AND METHOD**

(75) Inventor: **Hermann Ruckerbauer**, Moos (DE)

(73) Assignee: **Infineon Technologies AG** (DE)

(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 0 days.

(21) Appl. No.: **09/900,626**

(22) Filed: **Jul. 6, 2001**

(51) **Int. Cl.**[7] **G11C 7/00**
(52) **U.S. Cl.** **365/222**; 365/211
(58) **Field of Search** 365/222, 211, 365/228

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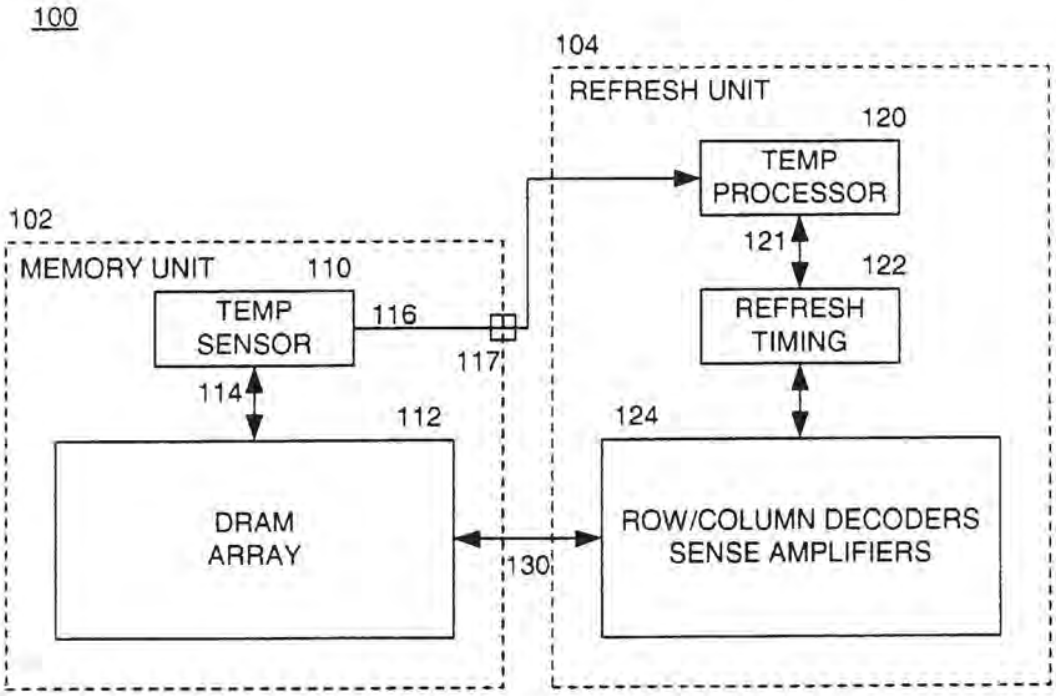
Primary Examiner—Vu A. Le
(74) *Attorney, Agent, or Firm*—Lerner, David, Littenberg, Krumholz & Mentlik, LLP

(57) **ABSTRACT**

An apparatus includes at least one dynamic random access memory (DRAM) array; and at least one temperature sensor in thermal communication with the DRAM array and operable to produce a signal indicative of a temperature of the DRAM array.

17 Claims, 5 Drawing Sheets



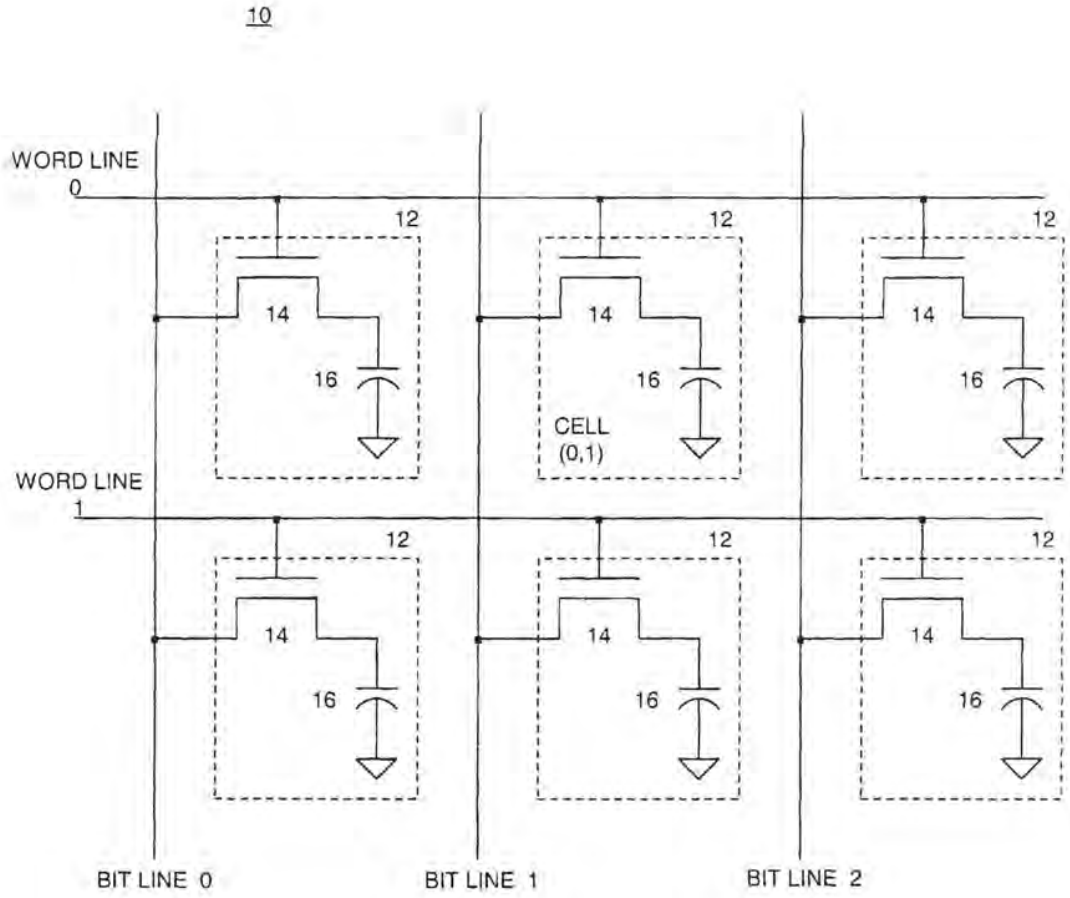

10
WORD LINE 0
WORD LINE 1
12
14
16
CELL (0,1)
BIT LINE 0
BIT LINE 1
BIT LINE 2

FIG. 1

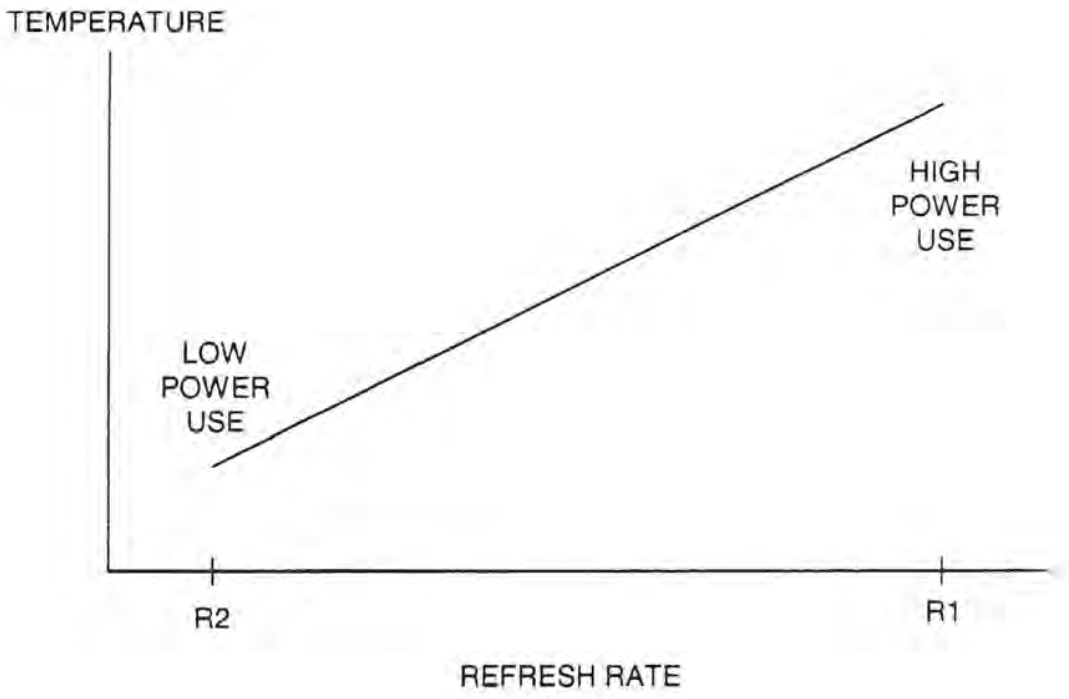


FIG. 2

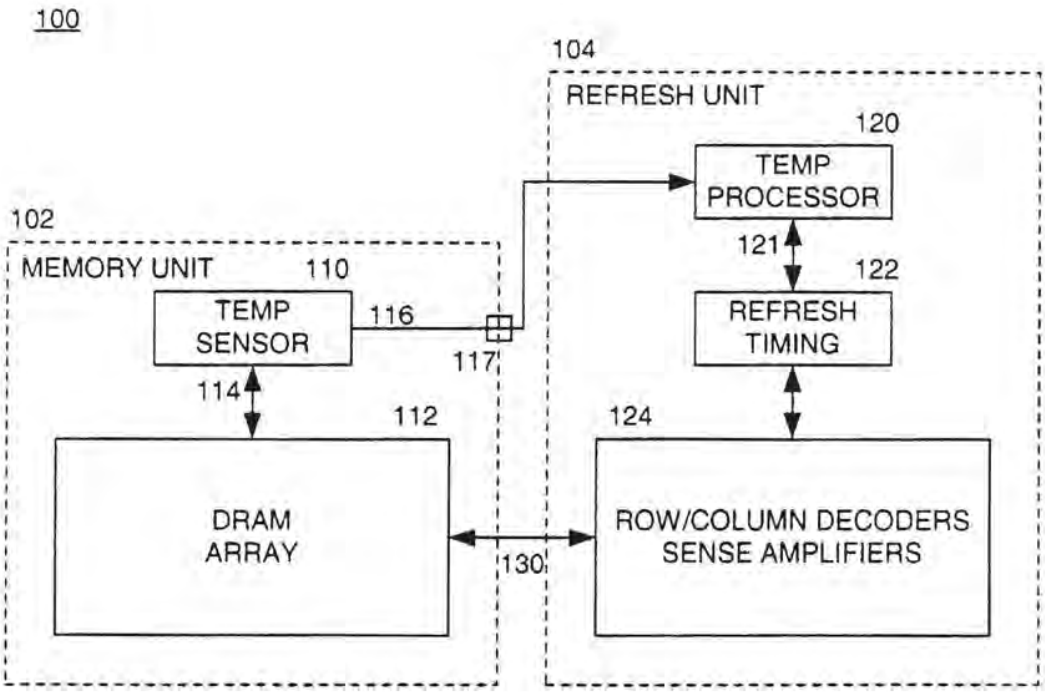

100
104
REFRESH UNIT
120
TEMP PROCESSOR
121
122
REFRESH TIMING
102
MEMORY UNIT
110
TEMP SENSOR
116
117
114
112
124
DRAM ARRAY
130
ROW/COLUMN DECODERS SENSE AMPLIFIERS

FIG. 3

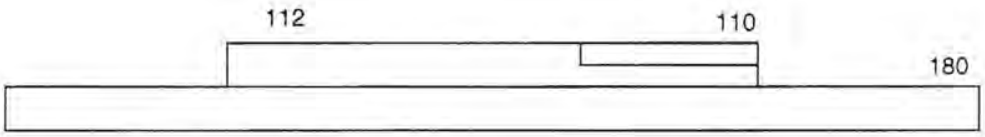


FIG. 4A

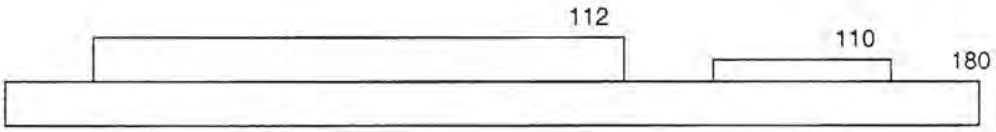


FIG. 4B

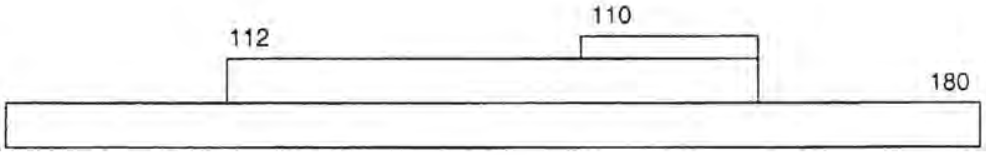


FIG. 4C

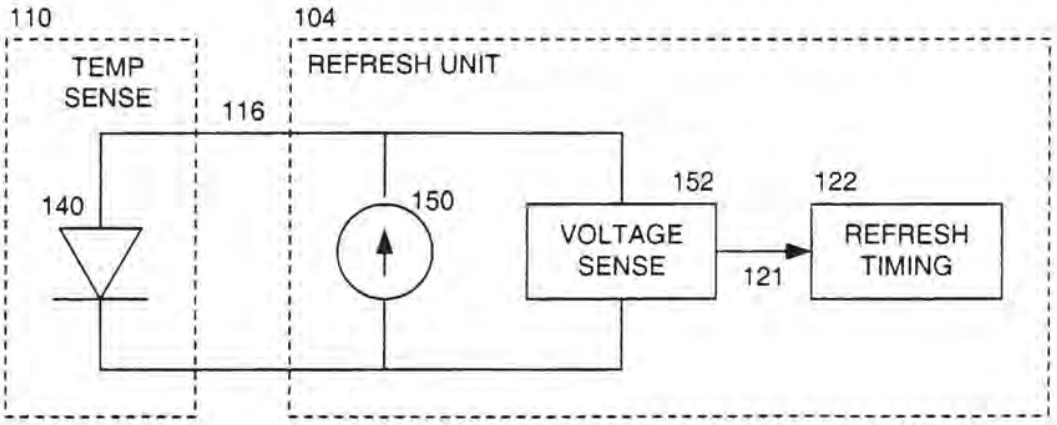

110
TEMP SENSE
104
REFRESH UNIT
116
140
150
152
VOLTAGE SENSE
121
122
REFRESH TIMING

FIG. 5

DRAM REFRESH TIMING ADJUSTMENT DEVICE, SYSTEM AND METHOD

BACKGROUND OF THE INVENTION

The present invention relates to devices, systems, and/or methods for refreshing the contents of a dynamic random access memory (DRAM) array and, more particularly, to devices, systems, and/or methods for utilizing a temperature of the DRAM array to adjust a refresh rate at which the contents of the DRAM array are updated.

A common form of random access memory (RAM) is dynamic random access memory (DRAM). With reference to the equivalent circuit shown in FIG. **1**, DRAMs employ a semiconductor technology called complementary metal-oxide-semiconductor CMOS to implement a memory array **10** including a plurality of memory cells **12**, each cell **12** consisting of a single transistor **14** and a single capacitor **16**. A given cell **12** of the DRAM array **10** may be accessed by activating a particular bit line and word line. As the cells **12** of the DRAM array are arranged in a grid, only one cell **12** will be accessed for each combination of word line and bit line.

For example, in order to write a data bit into cell **(0,1)**, word line **0** is activated by applying an appropriate voltage to that line, e.g., a logic high (such as 3.3V, 5V, 15V, etc.) or a logic low (such as 0V). The appropriate voltage on word line **0** will turn on each of the transistors **14** connected to that line including the transistor **14** of cell **(0,1)**. A voltage may then be presented on bit line **1**, which will charge the capacitor **16** of cell **(0,1)** to a desired level, e.g., a logic high or logic low consistent with the data bit. The voltage may be presented on bit line **1** (and/or any of the other bit lines) by way of a suitably connected data bus. When the voltage on word line **0** is removed, the transistor **14** of cell **(0,1)** is biased off and the charge on the capacitor **16** of cell **(0,1)** is stored.

Reading a data bit from a particular cell **12**, such as cell **(0,1)**, is substantially similar to writing a data bit except that the voltage on bit line **1** is imposed by the capacitor **16** of the cell **12** rather than by the data bus. Typically, a single cell **12** is not written to or read from; rather, an entire word (series of data bits) is written into the DRAM array **10** or read from the DRAM array **10** by applying the appropriate voltage on a particular word line and either imposing or sensing voltage on each of the bit lines **0**,**1**,**2**, etc.

Once data bits (i.e., voltages) have been stored on the capacitors **16** of the DRAM array **10**, the data are not permanent. Indeed, various leakage paths exist around the capacitors **16** and, therefore, failure to read the date may corrupt the stored voltages. In order to avoid the loss of data stored in the DRAM array **10**, the data are refreshed on a periodic basis. In particular, an external sense amplifier is employed to sense the data stored in the DRAM array **10** and rewrite (i.e., refresh) the data onto the capacitors **16**. Typically, the data associated with a particular word line (i.e., one data word) are refreshed every 7.8 microseconds (e.g., for 256 Mbit DRAM arrays) or every 15.6 microseconds (e.g., for 64 Mbit DRAM arrays). The refresh rate for a particular DRAM array **10** is established by the manufacturer and is based on a worst-case high temperature condition.

The refresh process may be implemented in either of two ways, namely, internally (self refresh) or externally (CBR or Ras only refresh). The internal refresh process requires that the DRAM itself set the refresh timing. The external refresh process requires an external chip (chipset) that issues a refresh command. The DRAM receives the refresh command from the external chip through a dedicated pin.

Unfortunately, the refresh process has a deleterious effect on overall system performance. Among these deleterious effects are: (i) an increase in power consumed by the DRAM array **10** and any external circuitry involved in the refresh process; and (ii) a decrease in overall system bandwidth. As to the former, the external sense amplifiers and other associated circuitry (e.g., row decoders, column decoders, etc.) involved in the refresh process, not to mention the DRAM array **10** itself, draw power in order to rewrite the data into the DRAM array **10**. In certain applications, such as in the automotive industry, power efficiency is desirable and increases in power consumption due to DRAM array **10** refresh cycles may be problematic. As to the latter, the refresh cycles of the DRAM array **10** take priority over routine reading and writing cycles and, therefore, the rate at which the DRAM array **10** is refreshed has a corresponding impact on the bandwidth (e.g., data throughput) of the overall system in which the DRAM array **10** is utilized.

Accordingly, there is a need in the art for a new device, system, and/or method for refreshing the data of a DRAM array such that power consumption is reduced and system bandwidth is increased.

SUMMARY OF THE INVENTION

In accordance with at least one aspect of the present invention, an apparatus includes: at least one DRAM array; and at least one temperature sensor in thermal communication with the DRAM array and operable to produce a signal indicative of a temperature of the DRAM array.

Preferably, the DRAM array is refreshed at a rate that varies in response to the signal. For example, the rate at which the DRAM array is refreshed may decrease as the temperature of the DRAM array decreases. Further, the rate at which the DRAM array is refreshed may increase as the temperature of the DRAM array increases.

Preferably, the at least one temperature sensor includes at least one diode having a forward voltage drop that varies as a function of the temperature of the DRAM array, and the signal corresponds to the forward voltage drop of the at least one diode. Alternatively, the at least one temperature sensor may be taken from the group consisting of thermocouples, thermistors, or any other device that provides an output signal that varies as a function of temperature.

In accordance with one or more further aspects of the invention, the apparatus may further include a refresh unit operable to refresh the DRAM array at a rate that varies in response to the signal. Preferably, the refresh unit includes a refresh timing unit operable to establish the rate at which the DRAM array is refreshed in response to the signal. It is preferred that the refresh timing unit is operable to decrease the rate at which the DRAM array is refreshed as the signal indicates that the temperature of the DRAM array decreases. It is also preferable that the refresh timing unit is operable to increase the rate at which the DRAM array is refreshed as the signal indicates that the temperature of the DRAM array increases.

When the at least one temperature sensor is a diode, it is preferable that the refresh unit is operable to sense the forward voltage drop of the diode to determine the temperature of the DRAM array.

In accordance with one or more further aspects of the present invention, the DRAM array and the at least one temperature sensor are disposed in a semiconductor package, the package including at least one connection pin operable to provide the signal to external circuitry.

In accordance with one or more further aspects of the invention, the DRAM array, the at least one temperature sensor, and the refresh unit are integrated in a semiconductor package.

In accordance with at least one further aspect of the present invention, the apparatus includes: at least one DRAM chip including the DRAM array and the at least one temperature sensor; at least one refresh chip operable to refresh the DRAM array at a rate that varies in response to the signal. Preferably, the refresh chip includes the refresh timing unit.

In accordance with one or more further aspects of the present invention, a method includes: sensing a temperature of a DRAM array; and refreshing contents of the DRAM array at a rate that varies in response to the temperature thereof.

The method preferably further includes decreasing the rate at which the DRAM array is refreshed as the temperature of the DRAM array decreases. The method may also include increasing the rate at which the DRAM array is refreshed as the temperature of the DRAM array increases. It is most preferred that the step of sensing the temperature of the DRAM array includes sensing a forward voltage drop of a diode that is in thermal communication with the DRAM array.

Other aspects, features, advantages, etc. will become apparent to one skilled in the art in view of the description herein taken in combination with the accompanying drawings.

BRIEF DESCRIPTION OF THE DRAWINGS

For the purposes of illustrating the invention, there are shown in the drawings forms which are presently preferred, it being understood, however, that the invention is not limited to the precise arrangements and/or instrumentalities shown.

FIG. **1** is a DRAM array in accordance with the prior art;

FIG. **2** is a graph illustrating the relationship between a temperature of the DRAM array and a desirable refresh rate of the DRAM array;

FIG. **3** is a block diagram of a DRAM apparatus in accordance with one or more aspects of the present invention; and

FIGS. **4A–4C** are structural views of alternative DRAM configurations in accordance with the present invention; and

FIG. **5** is a block diagram showing additional details of certain components of FIG. **3**.

DETAILED DESCRIPTION

With reference to FIG. **2**, it has been found that the refresh rate established by DRAM array manufacturers may be altered when the temperature of the DRAM array is lower than a worst-case value. For example, when the temperature of the DRAM array is relatively high, a correspondingly high refresh rate R1 may be required to ensure integrity of the data stored in the DRAM array. The relatively high refresh rate R1 unfortunately results in a correspondingly high power use and a low system bandwidth. Conversely, when the temperature of the DRAM array is relatively low, it has been found that a correspondingly lower refresh rate R2 may be utilized to ensure the integrity of the data stored in the DRAM array. Advantageously, the relatively lower refresh rate R2 results in a lower power usage and higher overall system bandwidth. Although the relationship between the temperature and the refresh rate of the DRAM array is illustrated as being a linear function in FIG. **2**, it is noted that the relationship may not be linear and may vary depending on the specific implementation of the DRAM array. It is believed, however, that the overall relationship between temperature and refresh rate for DRAM arrays will exhibit a positive slope. In accordance with one or more aspects of the present invention, this relationship is exploited to reduce power consumption of the DRAM array (and any associated circuitry) and improve overall system bandwidth.

FIG. **3**, is a block diagram of a system **100** for storing data in a DRAM array. The system **100** includes a memory unit **102** and a refresh unit **104**. The memory unit **102** preferably includes at least one temperature sensor **110** and at least one DRAM array **112**. The DRAM array **112** may be configured in a substantially similar way as shown in FIG. **1** and/or may be configured in accordance with any of the known technologies. Preferably, the temperature sensor **110** is in thermal communication with the DRAM array **112** (schematically illustrated by way of line **114**) and is operable to produce a signal on line **116** that is indicative of a temperature of the DRAM array **112**. By way of example, the DRAM array **112** may be implemented on a semiconductor chip and the temperature sensor **110** may be thermally coupled to the same semiconductor chip or to an intermediate member that is in thermal communication with the semiconductor chip.

The refresh unit **104** preferably includes a temperature processor **120**, a refresh timing unit **122**, and a decoder/amplifier unit **124**. The refresh unit **104** is preferably operable to refresh the DRAM array **112** (by way of connection **130**) at a rate that varies in response to the signal on line **116**. More particularly, the DRAM array **112** is preferably refreshed at a rate that decreases as the temperature of the DRAM array **112** decreases and/or refreshed at a rate that increases as the temperature of the DRAM array **112** increases. The temperature processor **120** is preferably operable to detect a level of the signal on line **116** and to provide an indication of the temperature (by way of line **121**) of the DRAM array **112** to the refresh timing unit **122**. The refresh timing unit **122** is preferably operable to establish the rate at which the DRAM array **112** is refreshed in response to the temperature indication from the temperature processor **120**. The row/column decoders and sense amplifiers **124** are preferably operable to perform the refresh function on the DRAM array **112** in accordance with known techniques at intervals dictated by the refresh timing unit **122**.

In accordance with at least one aspect of the present invention, the temperature sensor **110** and the DRAM array **112** are preferably disposed in a semiconductor package where the package includes at least one connection pin **117** operable to provide the signal on line **116** to external circuitry, such as the refresh unit **104**. In accordance with a further aspect of the present invention, the DRAM array **112**, temperature sensor **110**, and the refresh unit **104** are integrated in the same semiconductor package such that external circuitry is not required to perform the refresh function. In accordance with a further aspect of the present invention, the refresh unit **104** is implemented by way of one or more semiconductor packages so as to form a chipset with the package containing the temperature sensor **110** and the DRAM array **112**.

Reference is now make to FIGS. **4A–4C**, which are structural views of alternative configurations of the DRAM array **112** and temperature sensor **110**. In FIG. **4A**, the DRAM array **112** is disposed on an intermediate member **180**, such as a substrate, a heatsink, etc. The temperature

sensor **110** is integrated with the DRAM array structure **112**, such as by implementing the temperature sensor **110** into the semiconductor material of the DRAM array **112**. As shown in FIG. **4**B, an alternative structural configuration is contemplated where the DRAM array **112** and the temperature sensor **110** are disposed on the intermediate member **180**, where the intermediate member **180** exhibits desirable thermal conductivity properties. Indeed, in this configuration it is preferred that the intermediate member **180** exhibits a low thermal resistance between the DRAM array **112** and the temperature sensor **110** such that an accurate measurement of the temperature of the DRAM array **112** may be obtained. The structural configuration shown in FIG. **4**C shows that the temperature sensor **110** may be coupled to the semiconductor device **112**, such as by bonding it to the semiconductor material of the DRAM array **112**.

With reference to FIG. **5**, the temperature sensor **110** preferably includes at least one diode **140** having a forward voltage drop that varies as a function of the temperature of the DRAM array **112**. The signal on line **116** preferably corresponds to the forward voltage drop of the diode **140**. By way of example, the refresh unit **104** may include a current source **150** operatively coupled to the diode **140** such that the diode **140** is forward biased. The refresh unit **104** may also include a voltage sensor **152** operatively coupled across the diode **140** such that the forward voltage drop across the diode **140** may be measured. The voltage sensor **152** preferably produces a value on line **121** indicative of the temperature of the DRAM array **112** vis-a-vis the forward voltage drop of the diode **140**.

Although the use of diode **140** is preferred, various other temperature sensing devices and techniques may be employed, such as the use of one or more thermocouples, thermistors, etc.

In accordance with at least one further aspect of the present invention, a method of refreshing the contents of a DRAM array may be achieved utilizing suitable hardware, such as that illustrated in FIGS. **3**–**5** and/or utilizing a manual or automatic process. An automatic process may be implemented using any of the known processors that are operable to execute instructions of a software program. In either case, the steps and/or actions of the method preferably correspond to the functions described hereinabove with respect to at least portions of the hardware shown in FIGS. **3**–**5**.

Although the invention herein has been described with reference to particular embodiments, it is to be understood that these embodiments are merely illustrative of the principles and applications of the present invention. It is therefore to be understood that numerous modifications may be made to the illustrative embodiments and that other arrangements may be devised without departing from the spirit and scope of the present invention as defined by the appended claims.

What is claimed is:

1. An apparatus, comprising:

a semiconductor package including at least one connection pin;

at least one dynamic random access memory (DRAM) array disposed within the package; and

at least one temperature sensor in thermal communication with the DRAM array, operable to produce a signal indicative of a temperature of the DRAM array, and coupled to the at least one connection pin such that the signal may be provided to external circuitry,

wherein the DRAM array is refreshed at a rate that decreases as the temperature of the DRAM array decreases and that increases as the temperature of the DRAM array increases.

2. The apparatus of claim **1**, wherein the at least one temperature sensor includes at least one diode having a forward voltage drop that varies as a function of the temperature of the DRAM array, and the signal corresponds to the forward voltage drop of the at least one diode.

3. The apparatus of claim **1**, wherein the at least one temperature sensor is taken from the group consisting of thermocouples and thermistors.

4. The apparatus of claim **1**, wherein the at least one temperature sensor includes a diode having a forward voltage drop that varies as a function of the temperature of the DRAM array; the at least one connection pin includes a first pin coupled to an anode of the diode and a second pin coupled to a cathode of the diode; and the signal corresponds to a potential voltage between the first and second pins.

5. The apparatus of claim **1**, wherein the at least one temperature sensor is taken from the group consisting of thermocouples and thermistors.

6. The apparatus of claim **1**, further comprising a refresh unit operable to refresh the DRAM array at a rate that varies in response to the signal.

7. The apparatus of claim **6**, wherein the refresh unit includes a refresh timing unit operable to establish the rate at which the DRAM array is refreshed in response to the signal.

8. The apparatus of claim **7**, wherein the refresh timing unit is operable to decrease the rate at which the DRAM array is refreshed as the signal indicates that the temperature of the DRAM array decreases.

9. The apparatus of claim **7**, wherein the refresh timing unit is operable to increase the rate at which the DRAM array is refreshed as the signal indicates that the temperature of the DRAM array increases.

10. The apparatus of claim **7**, wherein the at least one temperature sensor includes at least one diode having a forward voltage drop that varies as a function of the temperature of the DRAM array, and the signal corresponds to the forward voltage drop of the at least one diode.

11. The apparatus of claim **10**, wherein the refresh unit is operable to sense the forward voltage drop of the diode to determine the temperature of the DRAM array.

12. The apparatus of claim **6**, wherein the DRAM array, the at least one temperature sensor, and the refresh unit are integrated in a semiconductor package.

13. A dynamic random access memory (DRAM) chipset, comprising:

at least one DRAM chip including a DRAM array and at least one temperature sensor in thermal communication with the DRAM array, the at least one temperature sensor being operable to produce a signal indicative of a temperature of the DRAM array, the DRAM chip including at least one connection pin operable to provide the signal to external circuitry; and

at least one refresh chip operable to refresh the DRAM array at a rate that varies in response to the signal,

wherein the refresh chip is operable to (i) decrease the rate at which the DRAM array is refreshed as the signal indicates that the temperature of the DRAM array decreases; and (ii) increase the rate at which the DRAM array is refreshed as the signal indicates that the temperature of the DRAM array increases.

14. The apparatus of claim **13**, wherein the at least one temperature sensor includes at least one diode having a forward voltage drop that varies as a function of the temperature of the DRAM array, and the signal corresponds to the forward voltage drop of the at least one diode.

15. The apparatus of claim **14**, wherein the refresh chip is operable to sense the forward voltage drop of the diode to determine the temperature of the DRAM array.

16. A method, comprising:

sensing a temperature of a dynamic random access memory (DRAM) array;

outputting a signal indicative of the temperature of the DRAM array to external circuitry; and

refreshing contents of the DRAM array at a rate that (i) decreases as the temperature of the DRAM array decreases; and (ii) increases as the temperature of the DRAM array increase.

17. The method of claim **16**, wherein the step of sensing the temperature of the DRAM array includes sensing a forward voltage drop of a diode that is in thermal communication with the DRAM array.

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